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ANALOG AND DIGITAL CIRCUITS

Practical applications

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Introduction

Designed as an operational tool - support for (self) training activities, the book ,,Analog and digital circuits. Practical applications" aims to address a wide spectrum of problems and theoretical approaches, accompanied by real examples and practical applications based on the theoretical part.

The book is addressed primarily to students following study programs at the Faculty of Automation and Computer Science, who are in first contact with circuits for computer systems. At the same time, the issues addressed in the book, the theoretical content and practical exercises can serve as an invitation to all those interested in the study of analog and digital circuits used mainly in modern systems (teachers, researchers, students from other study fields, graduates, engineers of different specializations, etc.). The study material offers support to both students in the individual and group study within the laboratories, orienting them towards the efficient self-organization of their own activity, as well as to teachers in the optimization of the design-organization-evaluation processes, in order to ensure the quality of the university training.

The main objective of the "Analog and Digital Circuits" course is to provide specific information and to prepare students for projects using discrete electronic devices and analog and digital integrated circuits. This book uses, in an operational way, the contents of the "Analog and Digital Circuits" course, focusing mainly on creating learning opportunities, by providing various teaching tasks, exercises, analysis, reflections, questions and comments.

The topics are designed in an active and interactive way and include essential theoretical elements, approaches to conceptual clarifications and classifications, completed by applications and tasks. The structure of the book is gradual in complexity, starting from the presentation of basic signal types or basic semiconductor devices and reaching the description of analog circuits and digital circuits. The laboratory tasks are not so much an end in themselves, but occasions, means of orientation towards the exercise of the abilities, the capacities that the students will use later, as an indicator of their professionalization in engineering.

We hope that this paper will help in developing the specific way of thinking in the field of engineering, will expand the spirit of teamwork between students and will streamline communication, contributing to increasing the quality of university education.

Cluj-Napoca, 2020

The Authors

Content

LINEAR CIRCUITS WITH RC ELEMENTS

1. OBJECTIVES

This laboratory work has as purpose the experimental study of transmitting signals through linear circuits realized with RC elements, respectively the study of the RC high-pass filter and RC low-pass filter circuits.

2. THEORETICAL CONSIDERATIONS

2.1 RC high-pass circuit

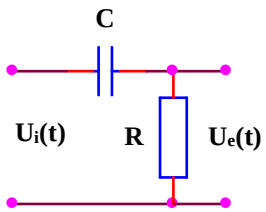

Fig.1.1

The RC high-pass filter (presented in Fig. 1.1), behaves like a voltage divider, having a dividing ratio that depends on frequency, the high frequency components of a non-sinusoidal signal applied at the input appear at the output with a smaller attenuation then low frequency components. In the extreme case, at zero frequency, the capacitance reactance becomes infinite, the continuous component of the signal is not transmitted at the output, resulting the usage of the RC high-pass filter for direct current circuits separation.

2.2 RC low-pass circuit

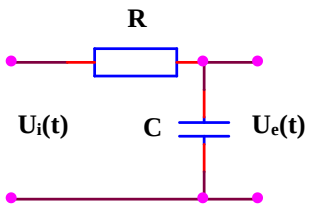

Fig.1.2

The RC low-pass filter (presented in Fig.1.2) behaves like a voltage divider, having a dividing ratio which depends on frequency, the low frequency components of a non-sinusoidal signal

applied at the input appearing at the output with a smaller attenuation than high frequency components.

3. PRACTICAL APPROACH

The study of the RC circuits will be done using the AIM-Spice simulation program.

3.1. We realize an RC high-pass filter using R = 1KΩ and C = 470nF.

3.2. Using a sin type stimulus, we will apply a sinusoidal signal having the period 1ms. The response of the circuit to this input signal will be displayed using the TR analysis. We will modify the value of the time constant of the circuit considering a higher, respectively a smaller time constant by modifying the value of the circuit's components. The analysis will be repeated observing the response of the circuit for the two cases. We will superimpose over the input signal a continuous component, observing the response of the circuit.

3.3. Using a pulse type stimulus, we will apply a rectangular signal having the period 1ms and the filling factor 50%. The response of the circuit to this input signal will be displayed using the TR analysis. We will modify the value of the time constant of the circuit considering a higher, respectively a smaller time constant by modifying the value of the circuit's components. The analysis will be repeated observing the response of the circuit for the two cases. We will superimpose over the input signal a continuous component, observing the response of the circuit.

3.4. We realize an RC low-pass filter using R = 1KΩ and C = 470nF.

3.5. Using a sin type stimulus, we will apply a sinusoidal signal having the period 1ms. The response of the circuit to this input signal will be

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3.6. Using a pulse type stimulus, we will apply a rectangular signal having the period 1ms and the filling factor 50%. The response of the circuit to this input signal will be displayed using the TR analysis. We will modify the value of the time constant of the circuit considering a higher, respectively a smaller time constant by modifying the value of the circuit's components. The analysis will be repeated observing the response of the circuit for the two cases. We will superimpose over the input signal a continuous component, observing the response of the circuit.

4. REPORT CONTENT

4.1. The short presentation regarding the characteristics of the RC high-pass filter and RC low-pass filter.

4.2. The layouts of the circuit, the tables with the computed values and the graphs of the plotted characteristics.

4.3. Observations concerning the nature of the differences between the theoretical values and the simulated results.

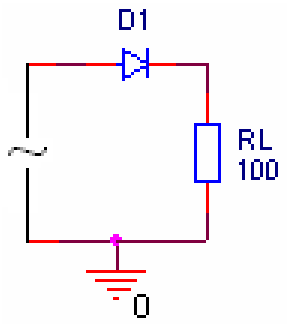
RECTIFIERS

1. OBJECTIVES

This laboratory work has as purpose the experimental study of half-wave and full-wave rectifiers.

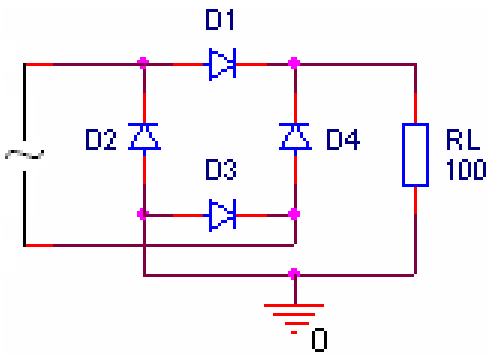
2. THEORETICAL CONSIDERATIONS

2.1 Half-wave rectifier



D_1 diode is on only when the anode's voltage is positive. In this way, positive alternations are allowed and negative alternations are blocked.

2.2 Full-wave rectifier



During positive alternations D_1 and D_3 diodes are on and during negative alternations D_2 and D_4 diodes are on. In this way, at the output only positive voltage will be obtained.

3. PRACTICAL APPROACH

The study of the rectifiers will be done using the AIM-Spice simulation program.

3.1. Mono alternating rectifier will be described.

3.2. Applying at the input a sinusoidal signal of 10V amplitude and 0V offset the output signal will be displayed.

3.3. Double alternating rectifier will be described.

3.4. Applying at the input a sinusoidal signal of 10V amplitude and 0V offset the output signal will be displayed.

4. REPORT CONTENT

4.1. Short presentation of the half-wave and full-wave rectifier characteristics.

4.2. The layouts of the circuit, the tables with the computed values and the graphs of the plotted characteristics.

4.3. Observations concerning the nature of the differences between the theoretical values and the simulated results.

CONTINUOUS VOLTAGE SOURCES

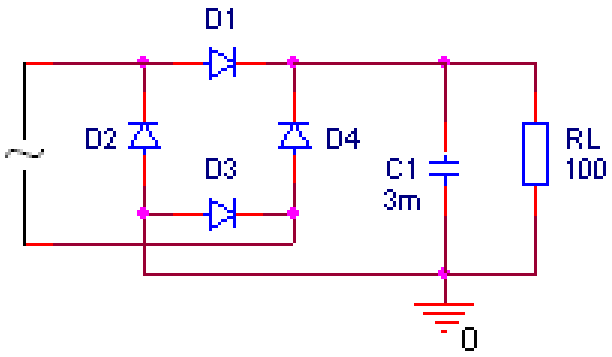
1. OBJECTIVES

This laboratory work has as purpose the experimental study of continuous voltage sources.

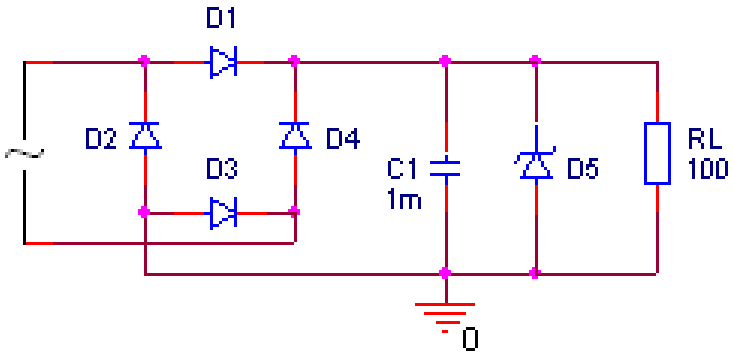
2. THEORETICAL CONSIDERATIONS

2.1 Filter rectifier

The capacitor stores energy during the time intervals in which the voltage supplied by the rectifier is greater than the voltage between the capacitor's plates and releases energy during the time intervals in which the voltage supplied by the rectifier is lower than the voltage between the capacitor's plates.



2.2 Parametric regulator with Zener diode

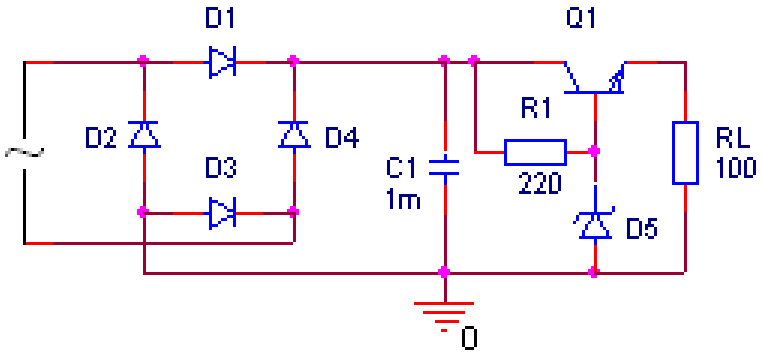


The functionality of the regulator is based on the Zener diode non-linear characteristic that

allows large current variations at small reverse polarity voltages applied on the diode.

2.3 Reaction regulator with no error amplifier

Increasing v_{OUT} voltage will determine the decrease of v_{BE} voltage, that in turn will determine the increase of v_{CE} and as a consequence v_{OUT} voltage will decrease. Similar, the v_{OUT} voltage decrease will determine the increase of v_{BE} voltage, that in turn will determine the decrease of v_{CE} voltage and as a consequence v_{OUT} voltage will increase. The regulator output voltage value is $v_{OUT}=v_Z-v_{BE}$.



3. PRACTICAL APPROACH

The study of the continuous voltage sources will be done using the AIM-Spice simulation program.

3.1. The circuits' schematics will be described.

3.2. Applying at the input a sinusoidal signal of 8V amplitude and 0V offset the output signal will be displayed. The analysis will be made accordingly to different values for the filtering capacitor and for the resistor.

4. REPORT CONTENT

4.1. Short presentation of the continuous voltage sources.

4.2. The layouts of the circuit, the tables with the computed values and the graphs of the plotted characteristics.

4.3. Observations concerning the nature of the differences between the theoretical values and the simulated results.

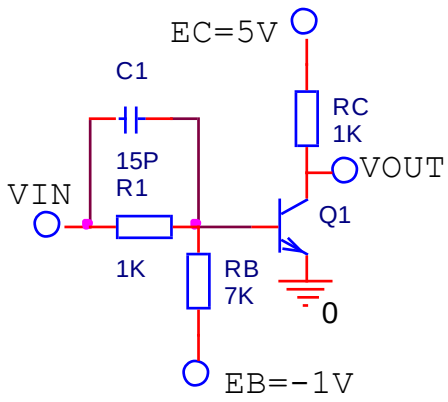
INVERTER WITH BIPOLAR TRANSISTOR

1. OBJECTIVES

This laboratory work has as purpose the experimental study of the inverter with bipolar transistor.

2. THEORETICAL CONSIDERATIONS

2.1 Inverter with bipolar transistor



If VIN is 0V, corresponding to 0 logic level, Q1 transistor is off and VOUT voltage will have 5V value, corresponding to 1 logical level. If VIN is 5V, corresponding to 1 logical level, Q1 transistor is on and VOUT voltage will have 0,2V value, corresponding to 0 logic level.

3. PRACTICAL APPROACH

The study of the inverter will be done using the AIM-Spice simulation program.

3.1. The layout presented in the paper will be described.

3.2. The static transfer characteristics of the inverter will be displayed.

3.3. The inverter dynamic behavior will be studied applying at the input a pulse type signal having 5MHz frequency. The analysis will be made accordingly to different values for the C1 capacitor: 1pF, 15pF and 47pF.

4. REPORT CONTENT

4.1. Short presentation of the inverter characteristics.

4.2. The layout of the circuit, the tables with the computed values and the graphs of the plotted characteristics.

4.3. Observations concerning the nature of the differences between the theoretical values and the simulated results.

TTL LOGIC CIRCUITS

1. OBJECTIVES

This laboratory work presents the constructive functioning characteristics of the TTL integrated circuit's family, and the main static and dynamic parameters of this circuit family.

2.THEORETICAL CONSIDERATIONS

2.1 Circuit functioning

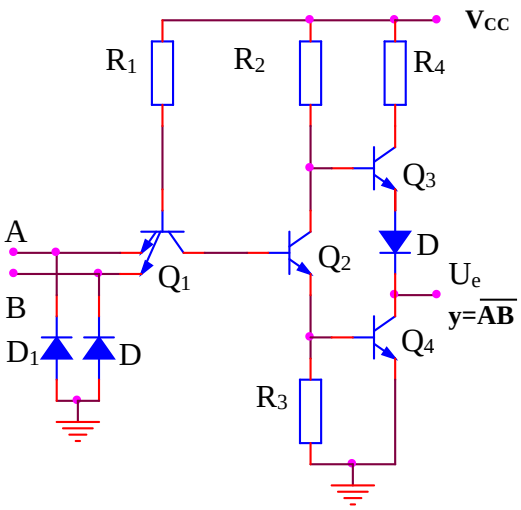


Fig.5.1

To show the electric functioning of the circuit in figure 5.1, let's assume first that one of the inputs is connected to the ground (logic level "0"). As a consequence, Q_1 transistor is saturated, and because of the voltage drop in it's collector, Q_2 transistor is cut-off stage. The low voltage in Q_2's emitter determines the blocking of the Q_4 transistor. The Q_3 transistor will be in conduction, being driven by the high potential in Q_2's collector. At the output we will obtain a high voltage, corresponding to "1" logic level.

If at both inputs we apply a voltage corresponding to "1" logic level, the basis-emitter junctions of the Q_1 transistor are reversed biased and the transistor works in the reverse active stage. In this case the basis-collector of the Q_1

transistor and the basis-emitter junctions of the Q_2 and Q_4 transistors form a chain of directly polarized diodes through the R_1 resistance from the plus of the voltage source. As a consequence the Q_3 and Q_4 transistors will become saturated. In the same time the Q_3 transistor is blocked because in it's basis there is a smaller potential than in it's emitter because of the voltage difference introduced by the D_3 diode. Thus we obtain at the output a potential equal to Q_4's collector-emitter saturation voltage which corresponds to "0" logic level.

If we analyze the functioning of the gate from the logical point of view, we observe that it realizes the NAND function, so: $C = \overline{A}\overline{B}$.

2.2 Circuit parameters

Logical levels: V_{ILmax} = 0.8 V, V_{IHmin} = 2 V, V_{OLmax} = 0.4 V, V_{OHmin} = 2.4 V and V_T = 1.3V

Noise margins: M_L = 0.4V and M_H = 0.4V

Input and output currents: I_{IH} = 40 μA, I_{IL} = -1,6 mA, I_{OH} = -800 μA and I_{OL} = 16 mA

Fan out: FO_L = 10, FO_H = 20 and FO = 10

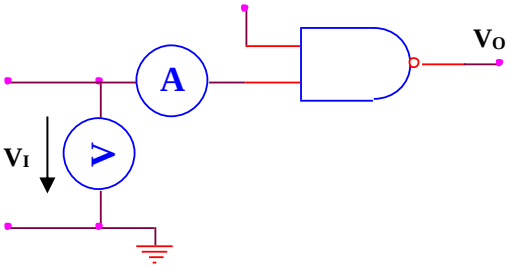


Fig.5.2

The input characteristic $I_I=f(V_I)$, can be obtained using the scheme in figure 5.2.

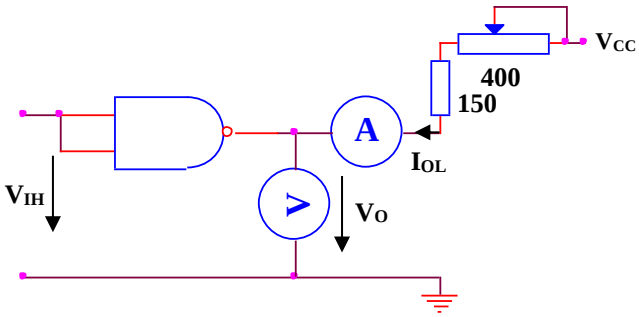


Fig.5.3

The output characteristic $V_{OL}=f(I_{OL})$ can be obtained using the scheme in figure 5.3 and the characteristic $V_{OH}=f(I_{OH})$ with the scheme in figure 5.4.

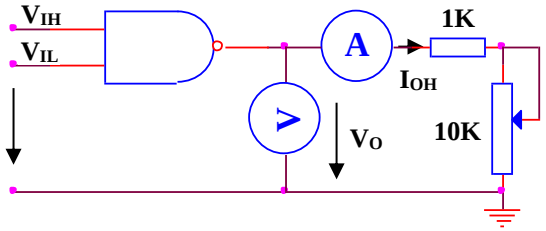


Fig.5.4

The short circuiting of the output to the ground can determine a current between 18 and 55 mA, through the Q_3 transistor, if Q_3, D_3 and R_4 work statically correct. This current is not dangerous if it has a short period. The variation of the short circuit with the supplying voltage

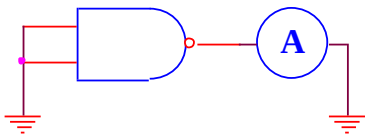


Fig.5.5

can be observed using the scheme in figure 5.5.

In the TTL integrated circuits family there are several series of circuits, which differ one from another by the compromise between the power consumption on the gate and the propagation time, as shown in the table below:

	74	74LS	74S	74ALS	74AS
Typical static power consumption/gate [mW]	10	2	19	1.2	8.5
Typical propagation time [ns]	10	9.5	3	4	1.5

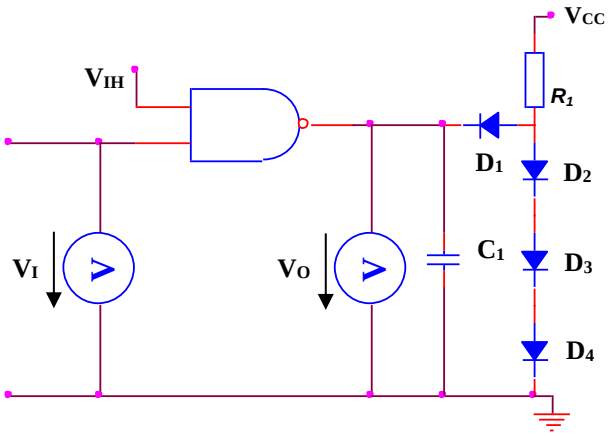


Fig.5.6

The transfer characteristic of the NAND standard gate can be plotted using the layout presented in figure 5.6. The circuit formed by R_1, D_1-D_4, connected to the gate output simulates an impedance equivalent to 10 TTL charges. The diodes are of 1N4148 type and C_1 includes the output capacitances of the probes and of the connecting system

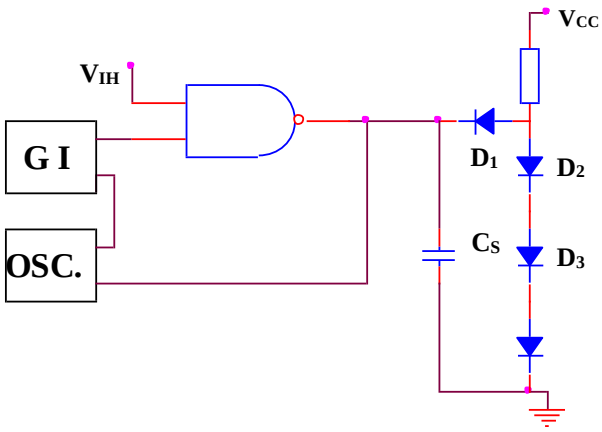


Fig.5.7

The dynamic characteristics of the TTL circuits can be determined using the circuit in figure 5.7, which simulates the loading of a gate with 10 TTL charges. The rising and falling times t_r and t_f have the typical values 8ns and 5ns respectively. The propagation time have the following typical values: t_{pHL}=8ns, t_{pLH}=12ns and t_p=10ns.

3. PRACTICAL APPROACH

3.1. Using the circuit in figure 5.6, the transfer characteristic of the TTL gate is plotted. The guaranteed output levels function of the admissible input voltage levels are checked.

3.2. Using the circuit in figure 5.2 the input characteristic is plotted.

3.3. Using the circuit in figure 5.5 the short circuit current of the fundamental TTL gate is determined.

3.4. Using the circuit in figure 5.1, if one input is kept at 5V and the other one is changed between 0V and 5V and then between 5V and 0V, the current absorbed from the voltage supply is viewed.

3.5. Using the circuit in figure 5.1, if one input is kept at 5V and the other one is changed between 0V and 5V and then between 5V and 0V the voltages in the entire circuit are viewed. Based on this graphs the circuit's functioning will be explained.

3.6. Using the circuit in figure 5.7 the dynamic behavior of the circuit will be analyzed.

4. REPORT CONTENT

4.1. The brief presentation of the TTL circuits' characteristic.

4.2. The schemes of the circuits, the tables with calculated values and the graphs representing the plotted characteristics.

4.3. The graphs obtained at the analysis of the TTL circuits' dynamic behavior.

4.4. Remarks on the nature of the differences between the theoretic values and the simulated results..

NMOS INTEGRATED CIRCUITS

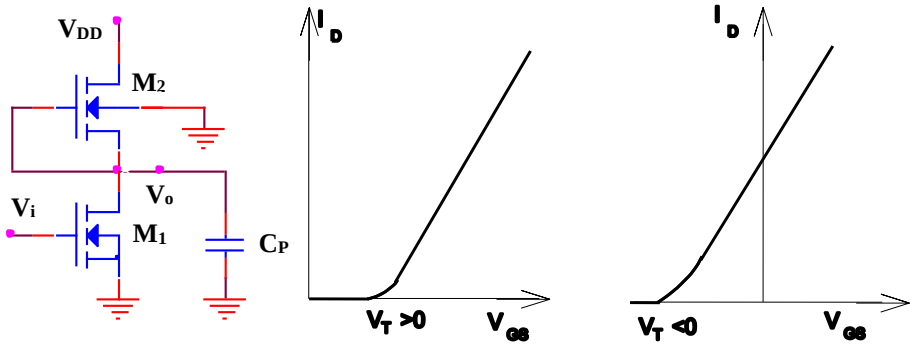
1. OBJECTIVES

In this laboratory work are presented the constructive functional characteristics of the family of NMOS integrated circuits and the main static and dynamic parameters of this family.

2. THEORETICAL CONSIDERATIONS

2.1 The NMOS static inverter

The layout of the NMOS static inverter is given in figure 6.1a.



a) b) c)

Fig.6.1

The M_1 transistor is an **n** channel enhancement mode transistor and has the input characteristic in figure 4.1b, and the M_2 transistor is a depletion mode transistor, having the input characteristic in figure 4.1c. This implies the threshold voltages V_T of the two transistors to be different, for M_1 the threshold voltage V_{T1} will be positive, and for M_2, the threshold voltage V_{T2} will be negative.

The circuit presents an inverter obtained with the M_1 transistor, in which M_2 works as an active resistance, replacing a fixed resistance. The external load of this inverter is generally made up also of inputs of NMOS transistors, which have a very large input resistance, therefore the load has practically a character of capacitance.

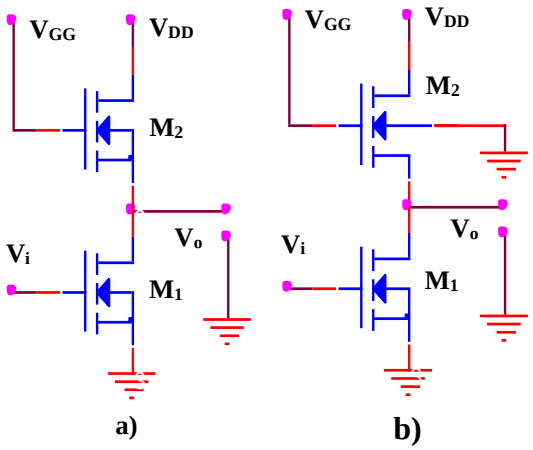


Fig.6.2

In figure 6.2 are considered two cases of connecting the substrate terminals of the load transistor M_2: the first case corresponding to binding the substrate terminal to the source terminal, and the second to binding the substrate terminal to a fixed potential.

In case the M_1 transistor conducts, in order to have at the output a potential as close to zero as possible, it is necessary for the transition resistance of the load transistor M_2 to be much greater then the transition resistance of the M_1 transistor. To satisfy the relationship between the transition resistances of the two transistors, the dimensions of the induced channel have to be correspondingly chosen for the M_1 and M_2 transistors, according to the relation: $\frac{W_1 / L_1}{W_2 / L_2} >> 1$.

If the inverter transistor M_1 is in cut-off stage, for the case in figure 6.2a, the output voltage will be:

$$V_o = V_{GG} - V_{T2}$$

For $V_{GG} = V_{DD} = 15V$ and $V_T = 4V$, it follows that $V_o = 11V$.

In order to have at the output a potential approximately equal to V_{DD}, the voltage applied on the gate of the M_2 transistor should be increased with the value of the threshold voltage V_T. In the given example $V_{GG} = V_{DD} + V_T = 19V$.

If the M_1 transistor is in cut-off stage, for the case in figure 6.2b, the output voltage will depend on V_{GG} and the threshold voltage, following a relation that contains also elements (parameters) specific to the intrinsic structure of the basis substrate. For higher threshold voltages, the value of the output voltage will decrease. For this reason, in order to ensure the logical levels at the output, we try to reduce the threshold voltage through technological procedures of fabricating the MOS transistors.

2.2 The static NAND gate

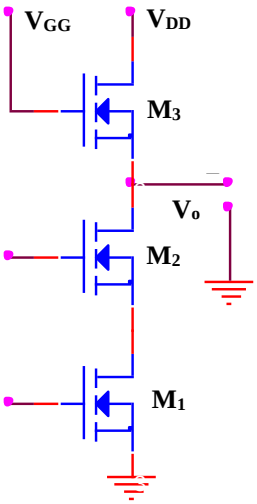


Fig.6.3

Figure 6.3 represents the static NAND gate realized with NMOS transistors. It contains two NMOS transistors, M_1 and M_2. On the gate of these transistors we apply the input signals; the transistors are connected in series. As a load resistance we use the M_3 transistor. In order to ensure the logical levels at the output, especially a lower level of the output voltage, sufficiently close to the ground, it is necessary for the active resistance to be 20 times greater then the transition resistance of the input transistors; because of this, the series connection of many transistors is not recommended.

The following values for the logical levels are considered: $V_L = 0V$ and

$V_H = V_{DD}$.

The functioning of the gate is the following:

- - if at both inputs we apply a voltage greater then the threshold voltage V_T, more precisely $V_{IH} = V_{DD}$, both M_1 and M_2 transistors conduct, and at the output the lower voltage level is obtained ($V_L \approx 0V$)
- if at least at one input a voltage smaller than V_T (usually V_{IL}=0V) is applied, the corresponding input transistor goes in cut-off stage and at the output the higher voltage level is obtained. At the output of the gate the NAND logical function is thus obtained: $F = \neg(A \cdot B)$

2.3 The static NOR gate

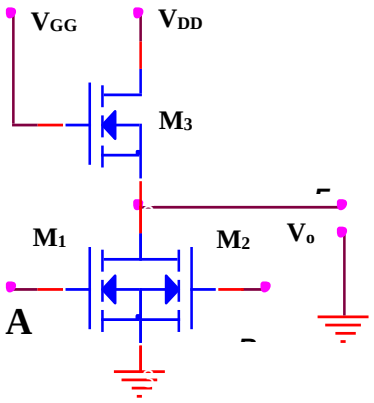


Fig.6.4

Figure 4.4 represents a NOR gate with NMOS transistors, composed by the parallel connection of the transistors on which the logic signals are applied at input. The load resistance is realized also with a NMOS transistor.

The functioning of the gate is the following:

- if on both inputs a lower voltage than the threshold voltage V_T (V_{IL} = 0V) is applied, the transistors M_1 and M_2 are in cut-off stage and at the output the higher voltage level $V_o = V_{OH} = V_{DD}$ is obtained.

- if at least on one input a voltage higher then the threshold voltage V_T is applied, so $V_{IH} = V_{DD}$, that transistor conducts, and at the output the lower voltage level $V_{OL} \approx 0V$ is obtained.

3. PRACTICAL APPROACH

3.1. Construct, with the aid of the circuit in figure 6.1a, the transfer characteristic of the NMOS inverter for different supplying voltages. Next verify the guaranteed levels for the output, function of the voltage values allowed for the input. Visualize the states of the two transistors if the input is driven with signal between 0V and V_{DD}.

3.2. Modify the threshold voltage of the two transistors and repeat the steps from point 3.1.

3.3. Using the circuit in figure 6.2a construct the transfer characteristic of the NMOS inverter for different transition resistances of the two transistors observing their influence on the behavior of the circuit.

3.4. Analyze the influence of the load on the logical levels of the circuit. Consider a load resistance R_S which will be connected to the ground and measure the voltage V_{OH}, then R_S will be connected to V_{DD} and measure the voltage V_{OL}.

3.5. Analyze the functioning of the inverter in dynamic regime. For this apply on the input of the circuit impulses with the amplitude equal to V_{DD} and follow the response, measuring the switching times in void and for C_S=0,5nF. Analyze the way the power consumption and the switching times are influenced by the supplying voltage variation. Analyze also the variation way of the power consumption function of the working frequency.

3.6. Repeat the steps before for the other gates shown in the laboratory work.

4. REPORT CONTENT

4.1. Briefly discuss the characteristics of the NMOS circuits.

4.2. The designs of the circuits, the tables with the computed values and the plots representing the constructed characteristics.

4.3. The plots obtained in the analyzing of the NMOS circuits dynamic behavior.

4.4. Remarks upon the nature of the differences between the computed theoretical values and the simulated results.

CMOS INTEGRATED CIRCUITS

1. OBJECTIVES

This laboratory work intends to study the static and dynamical characteristics the CMOS integrated circuits and special features in the use of CMOS circuits.

2. THEORETICAL CONSIDERATIONS

2.1. CMOS inverter

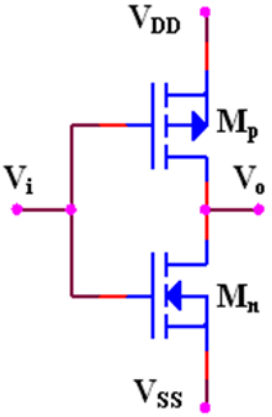


Fig.7.1

In the figure 7.1 a pair of MOS transistors is presented, one channel n and one channel p, which represents a CMOS inverter. This is the fundamental element on which logic gates are realized and any other functions needed in CMOS circuit design.

When a positive direct voltage ($+V_{DD}$) representing logic "1", is applied on common gates terminal, the NMOS transistor M_n opens and the PMOS transistor, M_p will be blocked. That ends with the output at the low voltage (V_{SS}) source, "0" logic.

In the same way, if a low voltage is applied on the common gate, the PMOS transistor (M_p) will be blocked and the NMOS transistor(M_n) will be opened. In this case, the output voltage will be at a high voltage ($+V_{DD}$), which is logic "1".

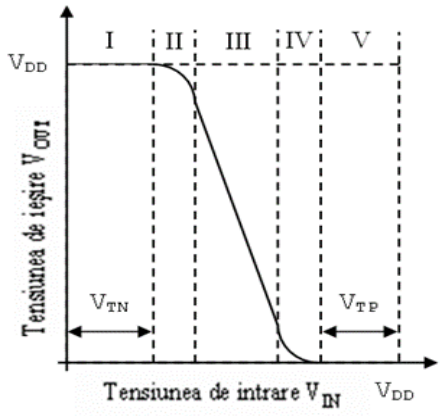


Fig.7.2

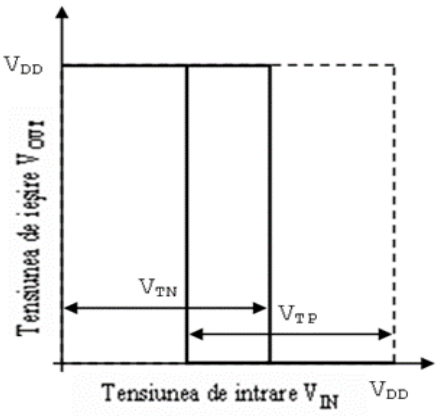


Fig.7.3

The transfer characteristic of the circuit is shown in the figure 7.2. This characteristic is dependent of the power supply voltage V_{DD}. This characteristic can be divided in five distinct regions in which the functioning of the transistors M_n and M_p is presented in the table below. V_{TN} is the threshold voltage of the NMOS transistor (M_n), and V_{TP} the threshold voltage of the PMOS transistor (M_p)

TENSIUNEA DE INTRARE V_{IN}	REGIUNEA	M_P	M_N
$0 \le V_{IN} \le V_{TN}$	I	LINIAR	BLOCAT
$V_{OUT} - \lvert V_{TP} \rvert \ge V_{IN} \ge V_{TN}$	II	LINIAR	SATURAT
$V_{OUT} - \lvert V_{TP} \rvert \le V_{IN} \le V_{OUT} + V_{TN}$	III	SATURAT	SATURAT
$V_{OUT} + V_{TN} \lvert \le V_{IN} \le V_{DD} - \lvert V_{TP} \rvert$	IV	SATURAT	LINIAR
$V_{DD} - \lvert V_{TP} \rvert \le V_{IN} \le V_{DD}$	V	BLOCAT	LINIAR

If the supply voltage V_{DD} is smaller than $V_{DDmin} = V_{TN} + \lvert V_{TP} \rvert$, the inverter will present a transfer characteristic with hysteresis, as shown in the figure 5.3 and the circuit cannot be used as a logic gate.

The typical value of threshold voltage on standard CMOS structures is:

$$V_{TN} = |V_{TP}| = 1.5V$$

hence V_{DDmin}=3V, the minimal value of supply voltage for CMOS.

Input and output logic levels:

- $V_{0Hmin}=V_{DD}$-0.5V (typical value: V_{DD} - 0.01V)

- V_{0Lmax}=0.05V (typical: 0.01V)

- V_{IHmin}=70%V_{DD}

- V_{ILmax}=30%V_{DD}

Noise margins:

$M_{ZL} = V_{ILmax} - V_{OLmax}$=30%$V_{DD}$

$M_{ZH} = V_{IHmin} - V_{OHmin}$=30%$V_{DD}$

In practical use, the noise immunity is about 45.50% of the supply voltage.

3. PRACTICAL APPROACH

3.1. The study of the CMOS logic gates, with the CMOS inverter presented in figure 7.1. Draw the transfer characteristic, determine the power consumption, and determine the states of the two transistors if at the input is applied a linear signal between 0V and V_{DD}. Determine logical levels between the two states and the threshold voltage for different supply voltages. The circuit behavior will be tested if the supply voltage is under 3V by drawing the static characteristic. Examine the influence of the output load upon logical states of the circuit. For this the load resistance R_S, needs first to be connected to the ground, then measure

V_{0H}, and then R_S needs to be connected at V_{DD}, and measure V_{0L}. In the same time there can be measured the conduction resistance of the transistors M_n and M_p. Measure the noise level margins and compare them with the granted levels at different values of the supply voltage.

3.2. Analyzing the circuit in dynamic regime. Apply at the input impulses with amplitude equal with V_{DD} and record the output, measuring the commutation times without load, and for C_S=0,5nF. Examine how power consumption and commutation times are influenced by supply voltage. Also, see how the working frequency influences the power consumption.

4. REPORT CONTENT

4.1. Short description of the CMOS inverter gate.

4.2. Schemes of the circuits, tables and calculated values with the graphics of the given characteristics.

4.3. Graphics obtained from the study of the dynamic regime of CMOS circuit.

4.4. Observations on the nature of the differences between theoretical values and the simulated values.

CMOS TRANSMISSION GATE

1. OBJECTIVES

This laboratory work intends to study the static and dynamical characteristics the CMOS integrated circuits and special features in the use of CMOS circuits.

2. THEORETICAL CONSIDERATIONS

2.1 Transmission gate

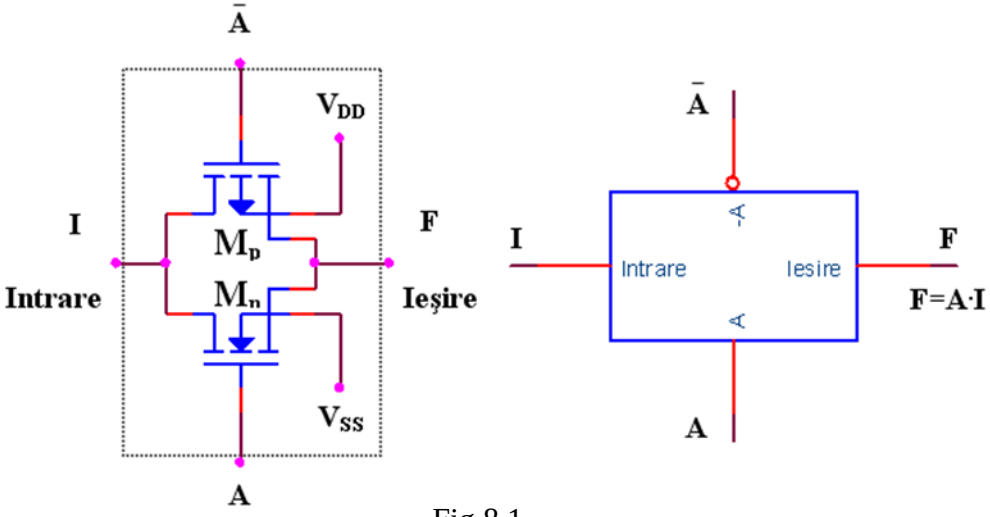


Fig.8.1

Another fundamental element in the CMOS construction is the transmission gate. It consists from a pair of complementary MOS transistor connected in parallel, like in the figure 8.1. The circuit acts like a switch, the logic variable A being the control input. When the control input A is in logic "1" and Ā in logic "0" the transmission gate is open, and between the input and output appears a small resistance which lets the current flow in any direction. The value of the input voltage must be positive related to V_{SS} and negative related to V_{DD}. When

A is in logic “0” and Ā is in logic “1”, the transmission gate is blocked, and there is a big resistance between the input and the output of the circuit.

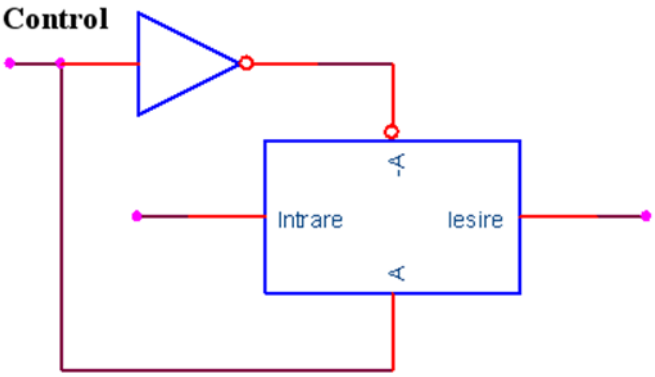


Fig.8.2

The transmission gate with an inverter forms a bilateral switch (figure 8.2).

Using transfer gates we can implement logic circuits. For example, if a=1 and b=1 the circuit from the figure 8.3 is actually an OR function. The resistance implies a power consumption in static regime if at least one gate is open.

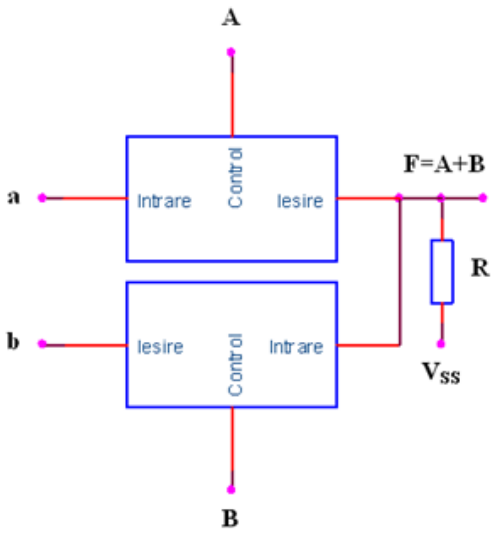


Fig.8.3

The OR gate can be realized without resistance if there are accessible at the input the additional command signals (8.4).

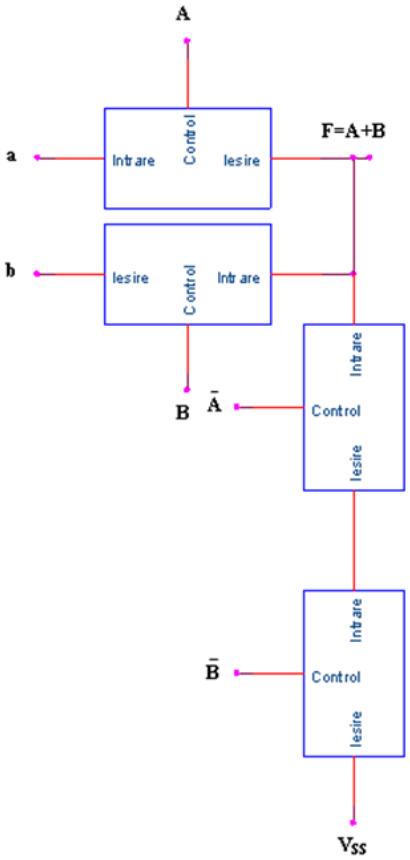


Fig.8.4

3. PRACTICAL APPROACH

3.1. Study the behavior of the transmission gates as bilateral switches for the transmission of the digital signals.

3.2. Realize the OR logic circuits with transmission gates and verify their OR function in static and dynamic regime.

4. REPORT CONTENT

4.1. Schemes of the circuits and their functioning.

4.2. Graphics obtained from the study of the static and dynamic regime of the circuits.

BUS DESIGN USING OPEN COLLECTOR LOGICAL CIRCUITS

1. OBJECTIVES

Open collector logical circuits will be studied and bus designing possibilities using wired function will be analyzed.

2. THEORETICAL CONSIDERATIONS

In order to connect several gates in parallel, open collector circuits or three state circuits are used.

In the electrical scheme of the open collector TTL gates the input level and the level separator used in the creation of the fundamental gate are not be changed. However, the output level has been modified, keeping only the Q_4 transistor (figure 9.1). In this case the collectors of the Q_4 transistors belonging to different circuits can be connected, the junction being connected through a resistance to the supply.

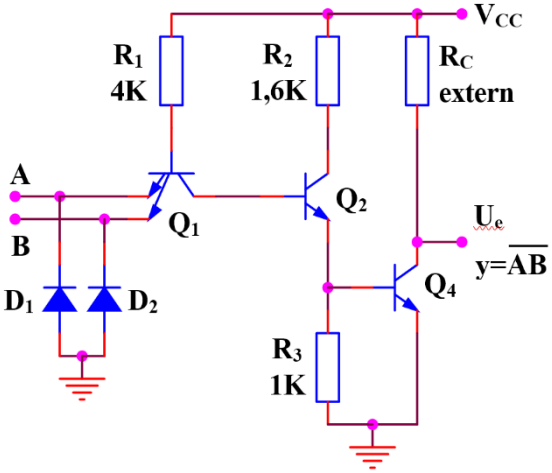


Fig.9.1

The common resistance is not included in the integrated structure and it's calculated by the scheme's designer depending on the number of the gates connected together (n) and

the number of the TTL gates that must be controlled by this common output (N).

The resistance R_c is calculated depending on the logical level of the common output, on the current generated by parallel connected gates and on the currents absorbed by the controlled gates.

In the case of 1 logical level at the output the result will be:

$$R_{c\max} = \frac{V_{cc\min} - V_{OH\min}}{n \bullet I_{OH\max} + N \bullet I_{IH\max}},$$

and for 0 logical level the result will be:

$$R_{c\min} = \frac{V_{cc\max} - V_{OL\max}}{I_{OL\max} + (n-1)I_{OH\max} - N \bullet I_{IL\max}},$$

The values of the charge resistances are calculated as following: V_{cc}=5V±5%, I_{OH}=250μA, I_{OL}=16mA, I_{IL}=1.6mA, I_{IH}=40μA, V_{OHmin}=2.4V, V_{OLmax}=0.4V.

To create, for example, the function implemented in figure 9.2 a three level logic is necessary, leading to a great delay. The same function can be implemented with open collector circuits. The function is denoted wired-AND.

$$f(A,...,F) = \overline{AB} \bullet \overline{CD} \bullet \overline{EF} = \overline{AB + CD + EF}.$$

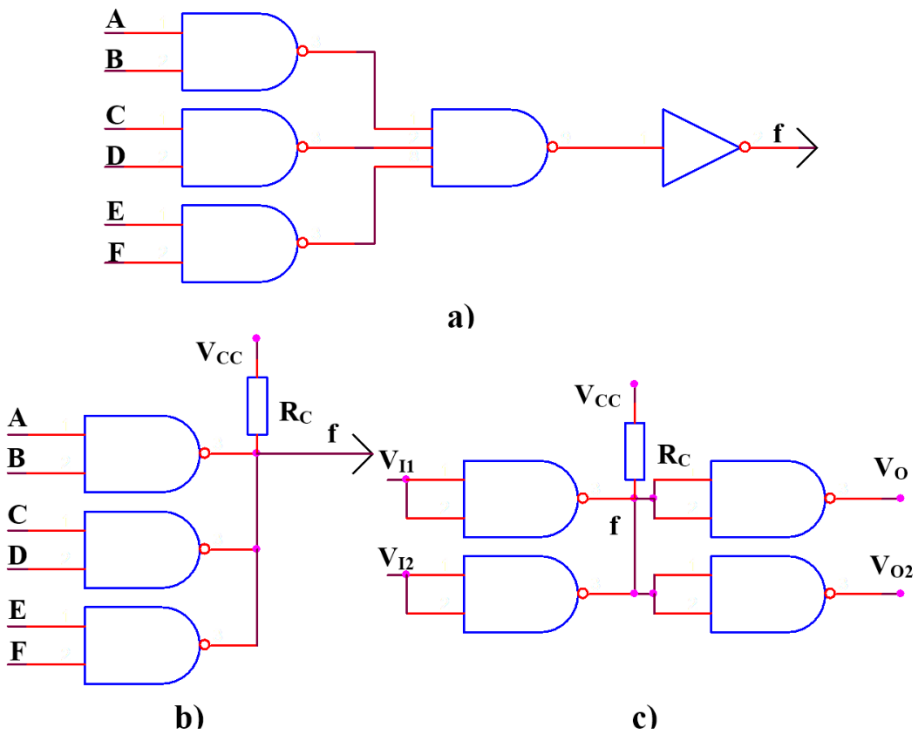


Fig.9.2

The circuit implements the AND function between the outputs of the NAND gates. The whole circuit implements the NOT-AND-OR for the group of variables at the input of the NAND gates

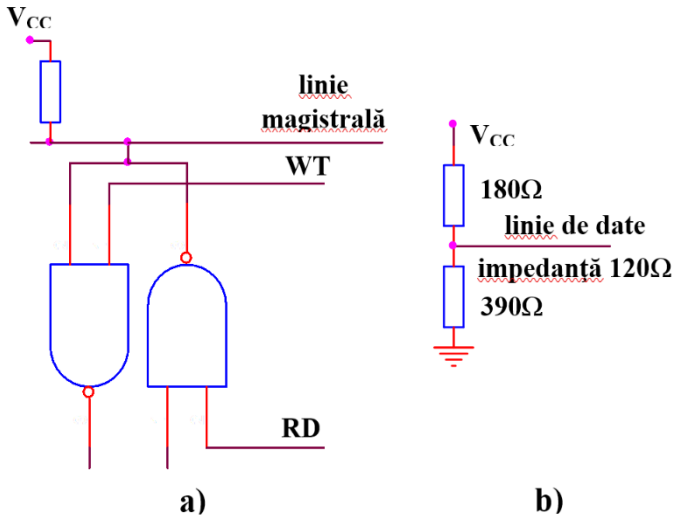


Fig.9.3

The open-collector and three-state circuits are

widely used for bus manufacturing. A circuit connected to a bus works, normally, both as an emitter and a receiver. For this reason, the command inputs have to allow both read and write operations from and on the bus. The word is introduced on the bus using when the RD command signal authorizes the operation. Through a WR command the word is fetched from the bus (figure 9.3.a). If only TTL circuits are connected to the bus, bus-terminators can be used (a group of resistances connected at the bus terminals to adapt against reflections) figure 9.3.b.

3. PRACTICAL APPROACH

3.1. The study of the open-collector gate (figure. 9.1) functioning using the circuit from figure 9.2.c. For a 1 logical state at the output increase R_c until V_{OH} decreases under 2.4V. Denote it by R_{cmax} and compare it with the computed one. For 0 logical at the output decrease R_c until V_{OL} is greater than 0.4V, denote it by R_{cmin} and compare it with the computed one. Repeat these operations for various charges.

3.2. Verify the truth table of the logical function realized by the circuit in the figure 9.2.b. Study the behavior of the circuit in dynamical regime by applying at the input a rectangular signal. Observe the behavior of the circuit when a capacitance of 2000pF is connected to the output.

3.3. Implement the circuit in the figure 9.3.a and analyze its dynamical and static behavior.

4. REPORT CONTENT

4.1. Brief description of the open-collector circuits.

4.2. Draw the circuits, the data tables and the graphical representations of

the studied characteristics.

4.3. Draw the charts obtained from the dynamical behavior of the circuits.

4.4. Remarks related to the difference between the theoretical computed values and the simulated values.

BUS DESIGN USING THREE STATE CIRCUITS

1. OBJECTIVES

Three state logical circuits will be studied and there will be analyzed the designing possibilities of the buses using this type of circuit.

2. THEORETICAL CONSIDERATIONS

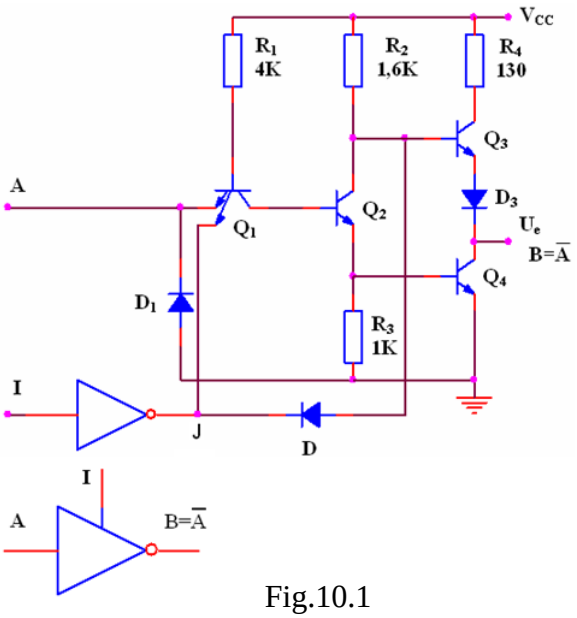


Fig.10.1

The impediments introduced by the external resistance necessary for open collector circuits are eliminated in the case of three state circuits (TSL - Three State Logic). In the output circuit of a TTL gate always one of the Q_3 or Q_4 transistors is on. If both transistors are off the output circuit is isolated and, seen from outside, the TTL gate presents an high impedance. Circuit has three states: 0 logical state, 1 logical state and high impedance, that leaves the output floating when both transistors are off.

The layout of an TTL inverter with three states is presented in figure 10.1.

Inhibiting input I allows for ordinary NOT gate behavior if I=0. If I=1, J=0, D is on, Q_1 is saturated, Q_2 and Q_4 are off, Q_3 is off because through opened D diode its basis potential decreases to 0.7V so the circuit will present at the output an high impedance (HZ).

In dynamic stage, beside the known propagation times t_{PLH} and t_{PHL} the following parameters appear:

- the time for high impedance establishment starting from 0 logical state t_{LZ}, and from 1 logical state respectively, t_{HZ};

- the time for exiting from high impedance state and going to 0 logical state, t_{ZL}, and going to 1 logical state respectively, t_{ZH}.

Considering these delays the total propagation time through these gates is around 25 ns. This value is larger than the one for usual TTL gates but is much smaller than the value for open collector circuits.

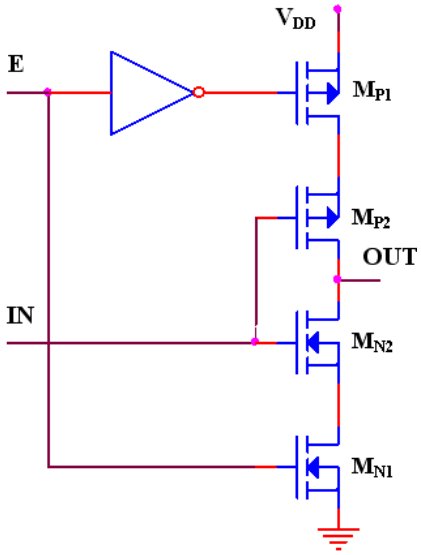


Fig.10.2

Also, in the case of CMOS gates output circuits that can have high impedance state are available. Such a circuit contains two n channel transistors and two p channel transistors (figure 10.2). A pair of p-n transistors operates with standard NOT function, and the second pair works as on-off switch driven by the enable input E.

If E input is in 1 logical state, M_{N1} and M_{P1} transistors are on and the output can

present 1 and 0 logical levels. When E input is in 1 logical state, the output impedance is high (higher than $10^{10}\Omega$ at 25°C)..

The open-collector and three-state circuits are widely used for bus manufacturing. A circuit connected to a bus works, normally, both as an emitter and a receiver. For this reason, the command inputs have to allow both read and write operations from and on the bus. The word is introduced on the bus using when the RD command signal authorizes the operation. Through a WR command the word is fetched from the bus (figure 10.3.a). If only TTL circuits are connected to the bus, bus-terminators can be used (a group of resistances connected at the bus terminals to adapt against reflections) figure 10.3.b.

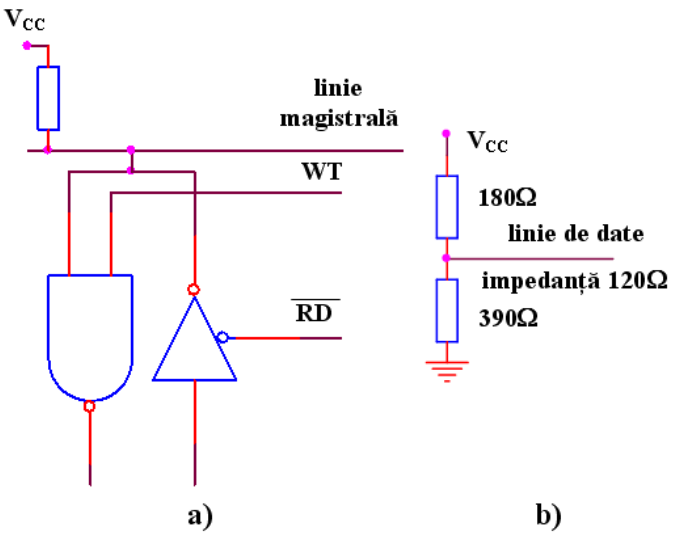


Fig.10.3

3. PRACTICAL APPROACH

3.1. The static parameters and the dynamic behavior of the three state TTL circuits will be studied. For static parameters study, I input is hold at 0V and A input is changed from 0V to 5V. For dynamic parameters study, a 15pF load is used.

3.2. The static parameters and the dynamic behavior of the three state CMOS

circuits will be studied. For static parameters study, E input is hold at 5V and IN input is changed from 0V to 5V. For dynamic parameters study, a 15pF load is used.

3.3. The circuits from figures 10.3 will be described and their behavior in static and dynamic stage is analyzed. Both TTL and CMOS circuits will be considered.

4. REPORT CONTENT

4.1. Brief presentation of three state circuits.

4.2. Circuits layout, tables with computed values and graphs representing the raised characteristics.

4.3. The graphs obtained by dynamical behavior analysis of the circuits. Observations on the nature of the differences between the calculated theoretical values and the simulated results.

MEASUREMENTS USING MULTIMETERS

1. OBJECTIVES

This paper studies the characteristics of the digital multimeter and shows how to measure the most important electrical elements.

2. THEORETICAL CONSIDERATIONS

The multimeter is one of the most used devices in electronics, with determination and measuring electrical quantities functions. With the development of integrated circuits, the digital multimeter appeared whose main difference from the analog display is how the result is displayed- in the liquid crystal display(LCD).

Measurable quantities with multimeter:

- electrical resistance- measuring unit Ohm (Ω);
- voltage – volt (V)
  - ❖ alternative voltage (~);
  - ❖ continuous voltage(=);
- intensity of electrical current – ampere (A);
  - ❖ direct current(=);
  - ❖ alternative current (~);

Besides these electrical quantities, multimeters also provides the opportunity to check how function some components, like (it can appear differences between different types of multimeters):

- resistance (by direct measurement on ohmic scale);
- semiconductor diode;

- electrical capacitance;
- bipolar transistors;

For describing how to work with the multimeter (figure 11.1) we will use the following notations:

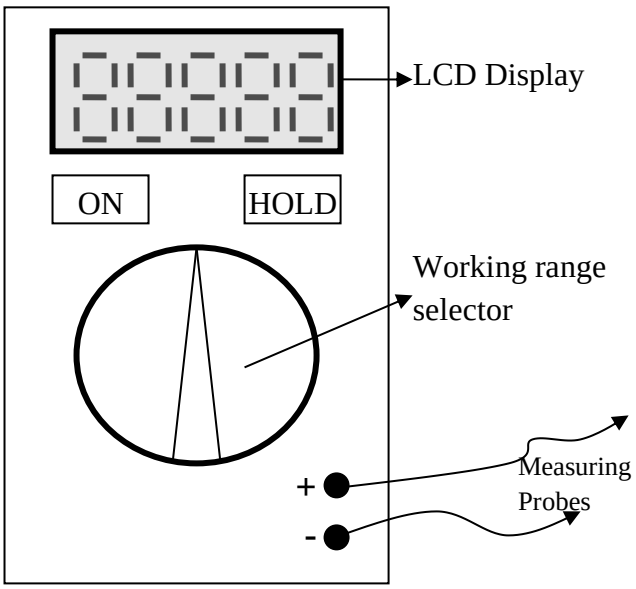


Fig. 11.1. Schematic presentation of a multimeter

- button ON - allows to start/ close the multimeter
- button HOLD - allows us to maintain the value showed on the display until pressing the button (the measurement can’t be made with the button pressed);
- working range selector- allows you to select the working mode of the device(measure quantities and determine the components) as well as the measuring range for electrical quantities.

Measurement circuits schemes using multimeter:

- **Voltages measurement**:

To measure the voltage (figure 11.2) the multimeter can be connected everywhere in the circuit, the value shown represents the voltage between those two test points.

Connection examples:

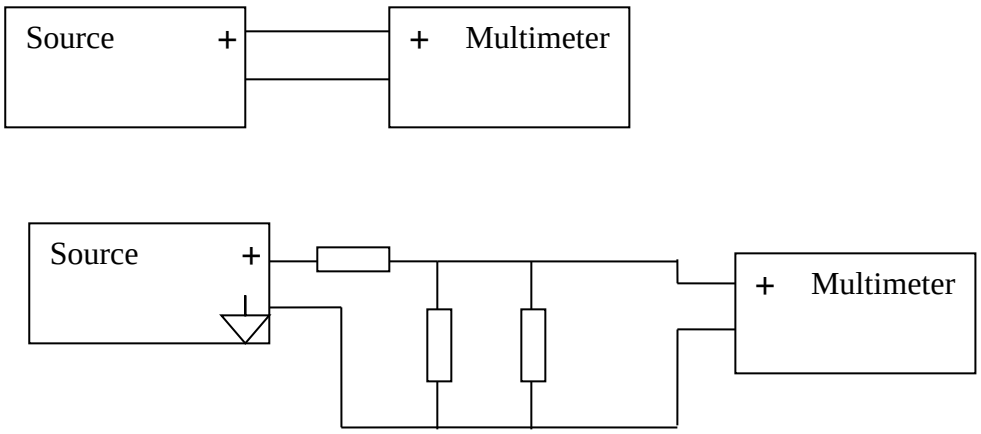


Fig. 11.2. Voltage measurement

DC voltage measurements (symbol V=)

We switch the range selector on one of the positions for DC voltage measurements. The selected inscription is the maximum amount which can be measured on that scale. The two cords must me connect the two points between which we want to measure the voltage, red cord represents + and the black cord is -.

Read the display. If voltage value is greater than the maximum of that scale, on the display we read 1 and change the switching range on a scale with

bigger values. If the displayed value is negative then the polarity of the measured voltage is reversed to the voltage corresponding to + at the red cord and – at the black one. If we switch the cords between them than the displayed value doesn't have sign, in this case we can say that the node where is connected the red cord has bigger potential.

AC voltage measurements V~

We switch the range selector to one AC voltage measurement positions and connect the measurement cords to the points of measurement. Then we read the displayed value, which represents the effective value of AC voltage measured.

Be careful when measuring the voltage at the outlet, so you don't get electrocuted!

- **Measurement of electrical currents**

When measuring the electrical current (figure 11.3), we must consider the following basic rules, before connecting the device:

- the red cord of the multimeter must be connected to the device' jack corresponding to the domain of measurement estimated (if we assume that there are large currents in the circuit, firstly we connect the terminal „Amps")

- always avoid shorting voltage sources with the multimeter. Current measurement is always made by inserting the resistance which determines the current, otherwise the multimeter is damaged (it burns!)

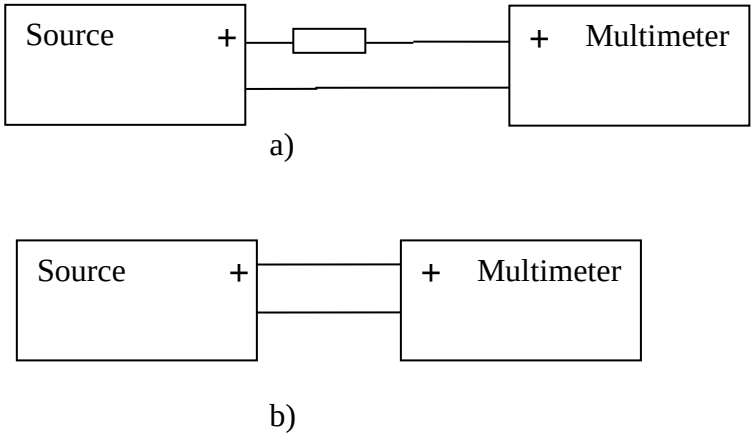


Fig. 11.3. Current measurement

a) Correct connection
b) Wrong connection of the device

- **Measurements of resistance**

On this scale the multimeter measures the electrical resistance between two points of the circuit or the electrical resistance of a component. We should mention that the value of a resistance is shown on it's body either in numerical value, either using the code of colors. In addition to we must also write the tolerance value, i.e. the maximum deviation (guaranteed by the manufacturer) of the real value of resistance from the nominal value.

With the range selector on a Ω position and the cord free the device indicates 1 (domain overflow, a normal thing considering that the electrical resistance between two wires in air is very big).

If the cords are shorted then the device must indicate 0, otherwise it means that the two probes are broken or the device battery is low.

The measurement of electrical resistance (figure 11.4) is made only in the absence of voltage or on separate components circuit. The measurement of a resistance placed in circuit can determine reading an erroneous value because of the electrical circuit loops.

Also, both hands are not held on the measuring probes because the resistance of the human body intervenes, connected in parallel with the measuring resistance.

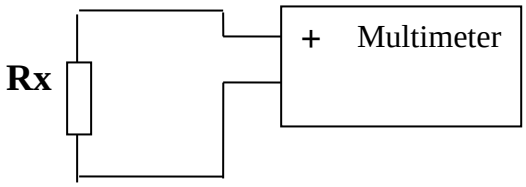


Fig. 11.4. Resistance measurement

- **Determine the functionality of semiconductor devices**

Also on the positions "Ohmmeter" is the position for checking the diodes and bipolar transistors. In direct sense, i.e. the red cord is on Anode and the black cord on cathode, the device indicates 0 or a small value, usually up to hundreds of ohms, and if we connect opposite the cords the device will indicate 1, that is field overtaking.

Bipolar transistors verification is made as if there were two diodes(diode base- emitter and base- collector diode).

For example, at an NPN transistors the red cord is connected to the base and we check the emitter and collector terminals to indicate a low resistance (hundreds of ohms). Put the black cord on base and the device must indicate a break at emitter and collector.

- **Determine the continuity of electrical paths**

Also on the ohmmeter scales is the position „buzzer" used for checking the electrical continuity between two points. If a short-circuit is made between the two cords of the device, a sound must be heard, in that moment we check only the device. Then the cords are positioned between the points we want to check the electrical continuity, if the device becomes noisy it means we have electrical continuity.

Continuity checking is always done in the absence of measuring circuit voltages, otherwise the device can be damaged!

- **Capacity measurements at capacitors(F)**

This function is found only on some digital multimeters, not being available on general ones (hobby).

We put the range selector o none of the positions for electrical capacity measurement. The capacitor is introduced in the special clamps for capacitors measure.

If the device doesn't have this function we can determine if we have a pierced capacitor by measuring it on the ohmic scale (very small resistance), but the measurement is not 100% sure, therefore is not recommended.

3. PRACTICAL APPROACH and REPORT CONTENT

1. Measure the values of the components and compare the measured values with the nominal values. Complete the following table for different resistances and capacitances:

Tolerance						

Nominal value						
Measured value						

2. Determine by direct measurement the voltage supplied to your mobile phones' battery or AC power. What influence has the measurement of a battery with de range selector on the position „Alternative voltage"?

3. Choose a resistance a o known value and connect it in series with the device and a battery with a known voltage. Measure the current in the circuit and check Ohm's Law.

4. Determine the anode at the provided diode and check if the diode are working or are damaged.

RC FILTERS. Practical assembly

1. OBJECTIVES

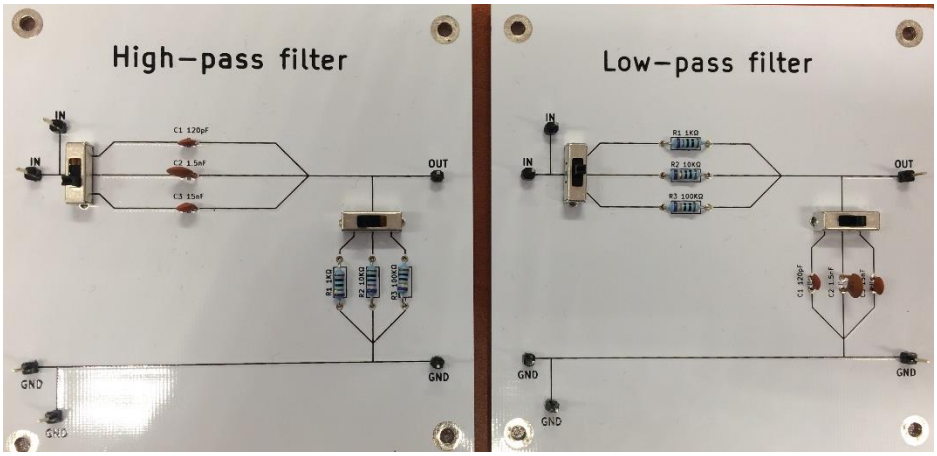
The purpose of this laboratory work is to study the RC filters simulated in a Laboratory 1 to determine the circuit response to various stimulus applied at its entry.

2. THEORETICAL CONSIDERATIONS

The study of the circuits behavior will be realized using the circuits provided and using the following devices:

- Function generator – rectangular and sinusoidal signal;
- Oscilloscope with 2 channels;
- Digital multimeter.

Given the practical aspect of the work, although the parameters that are determined are the same with those mentioned in the first Laboratory work, the course of the work will be changed.



The purpose of the work is to highlight the waveforms at the output of the circuits for the sinusoidal and rectangular signals applied at the input.

3. PRACTICAL APPROACH and REPORT CONTENT

1. Connect two oscilloscope measurement probes, power the oscilloscope and calibrate
   the two light paths, as follows:
   -The switch passes from each probe on the calibration position;
   -Select from the working mode of the oscilloscope to display both input channels (DUAL);
   -Attenuation of each channel is passed to 5V/div;
   -Both path of adjustment potentiometers (pos. Y) overlap the central mark of the oscilloscope display;
   -Both switches pass from the probe on position 1x (without attenuation);
2. Is selected channel 1 (Ch 1) as base time trigger of the oscilloscope at input;

3. The signal generator is powered and is set an AC sinusoidal output signal;
4. Connect probe 1 of the oscilloscope to the source output, according to the wires significance + (red wire from the source with the middle wire of the oscilloscope) and - (the mass);
5. Adjust the amplitude generated by the signal source to a maximum value of 5V (the peak amplitude measured on the oscilloscope should be a division, if the attenuation remains at 5V/div);
6. Oscilloscope attenuator is switching on a lower scale (1V/div) and monitors if the signal displayed is represented now on 5 divisions;
7. Both channels of the oscilloscope are passed on attenuation 5V/div and the calibration is restored;
8. Stop the signal source;
9. Connect the + terminal of the generator to the white wire of the board together with the + wire of the probe 1 of oscilloscope;
10. Connect mass (-) of the signal generator to the blue wire of the board, together with the – (mass) of the probe 1 and 2 of the oscilloscope ;
11. Connect + terminal of the probe 2 of the oscilloscope to the output 1 of the circuit (pine test is highlighted);
12. Power the signal generator;
13. From the range selector of the signal generator is set a starting frequency of approximately 150Hz, finely adjusting the potentiometer located on the front panel of the generator. WARNING: do not modify the signal amplitude!!!
14. From the control button of the oscilloscope time base (time/div) rotates until on the oscilloscope display we get a stable signal, representing some alternations of the input signal;

15. Draw the waveforms obtained, noting the value of frequency (read from generator), resistance and capacity (noted on components body) on 1:1 scale;
16. Click the button for generating the rectangular signal of the signal source and draw the waveform obtained;
17. Return to the sinusoidal signal and increase (from the adjustment potentiometer of source) signal frequency tracking the amplitude signal on channel 2 (on oscilloscope display) until these will start to decrease (Circ1 and Circ2 are low-pass filters, so with increasing frequency the amplitude of the output signal should decrease) . Notate the frequency at which peak to peak amplitude of the output signal has decreased with 1V (meaning 1 division on the oscilloscope display if the scale remained at 1V/div);
18. Draw the waveforms obtained on scale 1:1, highlighting how phase shift changed from the starting frequency;
19. Continue to increase the frequency and determine signals output amplitude and phase shift to a frequency of input signal of approximately 5kHz;

Repeat the above described steps for each of the other three assemblies on the board, highlighting cutting frequency and time constant of circuits. Also, at the filters 3 and 4 (FTS) highlight the lack of continuous component to output signal (it will be chosen from the signal generator an offset value of approximately 1V, pulling out the button and rotating the potentiometer slightly).

Remarks:

Changing the signal frequency provided from the signal generator

could lead to the loss of signal stability displayed on the oscilloscope or to display too many alternations on the screen, which makes difficult to trace the phase shifts and amplification. Since frequency represents the inverse of signals period, proceed as follows:

- once with the increase of the frequency generator will decrease the time base (time/div) of the oscilloscope.
- once with the decease of the frequency will increase the time base of the oscilloscope.

Oscilloscope signal period can be determined counting the divisions between two successive passages of the waveform through 0, determined on the X axis, and multiplying with the value displayed at time base switch (and after can be calculated the frequency).

Signals amplitude can be measured counting the divisions on the Y axis of the oscilloscope and multiplying with the attenuation indicated (V/div) of that channel.

THE STUDY OF BIPOLAR TRANSISTORS.
Practical assembly

1. OBJECTIVES

This work aims at the experimental study of circuits based on bipolar transistors: amplifier with bipolar transistor and inverter with bipolar transistor.

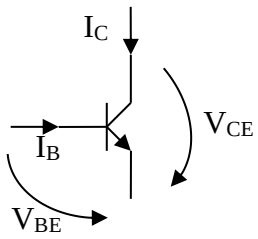
2. THEORETICAL CONSIDERATIONS

The bipolar transistor is an electronic device with amplification in current (the current between emitter and collector is determined by the base current). For this the transistor must by polarized correct, that is the junction base-emitter must be polarized direct and the junction base- collector must be polarized reverse.

Working modes of the transistor are:

Blocked transistor

The transistor is characterized in this situation by:



- $V_{BE} = 0$ V(the base – emitter tension is smallest than the opening tension of the junction) and $V_{CE} > 0$ – in this situation both junctions are blocked, so the current does not pass between emitter and collector.

- between emitter and collector appears o very high resistance : Ic - current of residual collector, of a very low value, of order μA;

- Ib – base 0 current.

The transistor in conduction

The transistor is characterized in this situation by:

- $V_{BE} > V_{BE0}$ (the opening voltage is specified in the catalog for that transistor) and

  $V_{CE} > V_{Cesat}$ (specified in the catalog) – in this situation the junction base – emitter is polarized direct, we have the base current I_B different from 0; the electrons whom reach from emitter in the base have a kinetic energy sufficiently large such as to "pass" the potential barrier of the emitter – base junction which is still polarized reverse;

- Between emitter and collector appears a resistance which is smaller and smaller, as the base current is growing, so the current established between emitter and collector is $I_C=\beta*I_B$. We say that the transistor is in the linear conduction area.

Saturated transistor

- $V_{BE} > 0.7V$, $V_{CE} = 0.2V$ (the values are de used ones, the real ones are specified in the catalog);

- as we increase the tension $V_{BE,}$ at some time moment it will be reach at the saturation of emitter – base junction and properly at the very strong increase of the base current (and implicitly the collector current). The tension V_{CE} is reaching a very low value, and the two junctions (base – emitter , emitter – base) are direct polarized. In this

situation, the collector current is limited only by the external resistances.

In case we want to amplify any signal it will be used the transistor in the linear region of the normal active regime and if we want to use it like am element of commutation (in logic circuits) it will be used in blocked – saturated regime.

1.AMPLIFIER WITH BIPOLAR TRANSISTOR

The correct polarization in case of use as an amplifier it is done usually with resistors whom values are chosen so that it is established a functioning regime in the linear area of the transistor, that is $I_C = \beta * I_B$, where I_C is the collector current, I_B is representing the base current, and β is the amplifying factor of the transistor (established from manufacturing).

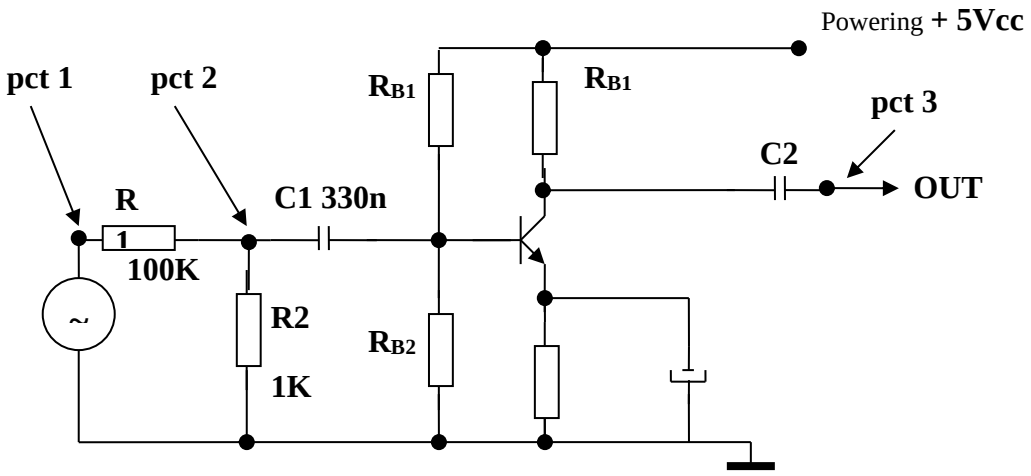
The circuit represented as follows includes the following blocks:

- an entrance attenuator realized with R1 and R2 resistors. This attenuator is in fact resistive

frequency divider introduced only because the signal sources in the laboratory do not allow to generate signals of low amplitude (until 1V).

- decouple capacitor C1 - allows the elimination of the continuous components of the input signal. This way is ensured only the amplification of the alternative component of the input signal (the useful component of the signal) this way the amplifier could enter in limitation.

You observe that " static operating point" it refers to the fact that in the absence of input signal, the transistor is opened, this is determined by direct measurement in the circuit of voltage drops.

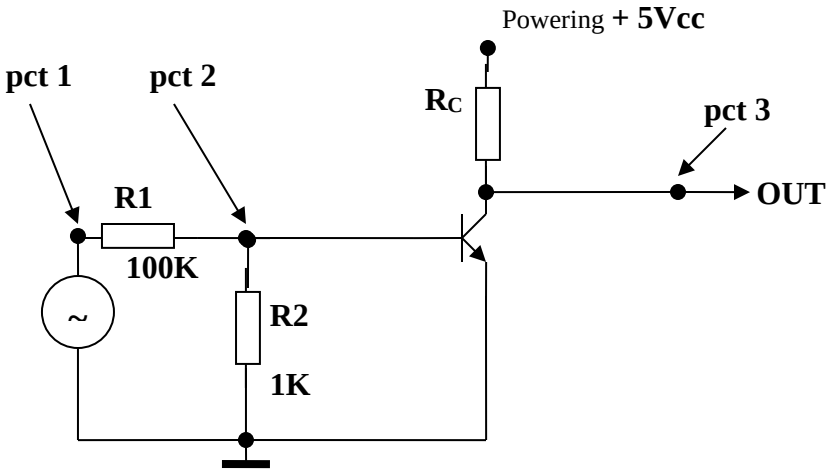


Electric scheme of amplifier

2.INVERTER WITH BIPOLAR TRANSISTOR

It is observed, in case of this circuit, the lack of any capacitors. This requires a much faster operating regime, at the expense of consumed power and the risk of destruction of components.

In this case we do not need the polarization circuit of the base because the transistor is used in "all or nothing" regime – blocked or saturated. The input circuit, realized with R_{B1} and $R_{B2,}$ is realizing a frequency divider, taking into consideration that the logical circuits are tension levels for "1" logic over 2V, which is dangerous to base-emitter junction.



Electric scheme of inverter

If V_{IN} has the value 0V, compatible to 0 logic level , the transistor is blocked and the tension V_{OUT} will have the maximum value, compatible to 1 logic level. If V_{IN} has the value 5V, compatible to 1 logic level, the transistor Q1 is opened and the tension V_{OUT} will have the value of about 0.2V, compatible to 0 logic level.

3. PRACTICAL APPROACH ȘI REPORT CONTENT

Study of the amplifier

- we power the stabilized supply and from the control potentiometer we adjust the value of 5V.

- with the multimeter we measure the terminal voltage source and then the supply stops;
- it is connected the stabilized supply at the powering wires (marked +5V and ground), taking into account the polarity (ground of supply to ground of the circuit);
- powering the power supply and with the multimeter measure the voltages across the junctions (base potential, emitter and collector in relation with the ground). Note these outages and determine the transistor state;
- the oscilloscope probe is connected to the signal generator **(attention: not at the stabilized power supply !!!!);**
- the source is powered and adjust it (watching the oscilloscope screen) to generate:
  - sinusoidal signal;
  - frequency of 5kHz
  - amplitude of 2V peak to peak
  - 1V continuous component
- connect the generator round to the montage ground and the + terminal is connected to the input of the test circuit;
- move probe 1 of the oscilloscope in test point 1 and probe 2 it input in test point 2. Note the amplitude difference between the signal applied at the input and that after the resistive divider!

- Move probe 1 of the oscilloscope in test point 2 and probe 2 in test point 3 (output of the amplifier)
- determine the amplification of the circuit, by comparing the output amplitude signal to signal amplitude in test point 2.
- increase the amplitude of the signal provided by generator. Up to what value of the test point 2 the output signal is correct amplified? Note the value!
- return to the amplitude of generated signal of 2V and change of the generated signal ;
- note the minimum frequency and the maximum frequency at which the amplification circuit is working properly.

Study of the inverter

- set the output voltage of the stabilized supply at a value of 5V;
- power the assembly;
- source signal is passed in working mode "TTL" and moves the probe to that output
- the generator is connected to input of the circuit. View the waveforms in test points. Determine the maximum operating frequency of the circuit!

80C51 MICROCONTROLLER FAMILY

1. OBJECTIVES

This paper examines the 80C51 microcontroller family and the specific design aspects of microcontroller-based systems.

2. THEORETICAL CONSIDERATIONS

Microcontrollers are integrated circuits, usually in CMOS technology, that incorporate various circuits required by a computer system. The 80C51 family of microcontrollers has the following features:

- 8051 central processing unit
    - 4k*8 ROM
    - 128*8 RAM
    - 3*16-bit counter/timers
    - Boolean processor
- External memory addressing capability
    - 64k*8 ROM (program)
    - 64k*8 RAM (data)
- 6 interrupts with 2 priority levels
- 4*8-bits I/O ports
- full–duplex UART
- asynchronous reset port

The integrated circuits in the microcontroller communicate by means of internal buses on which addresses, data or control signals can be conveyed as can be seen from the block diagram of the 80C51 microcontroller shown in figure 14.1.

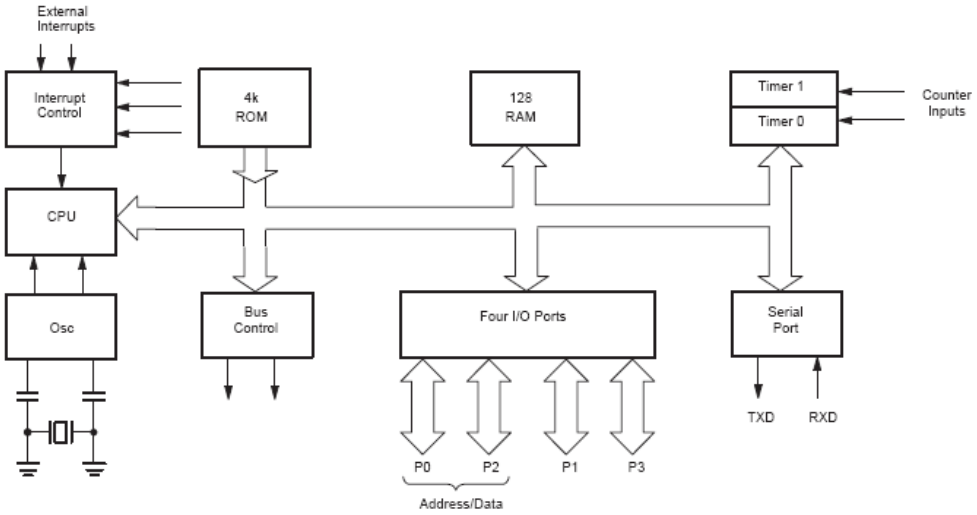


Figure 14.1 Block diagram of the 80C51 microcontroller

The logic symbol for the 80C51 microcontroller is shown in figure 14.2. The functions of the pins will be presented below.

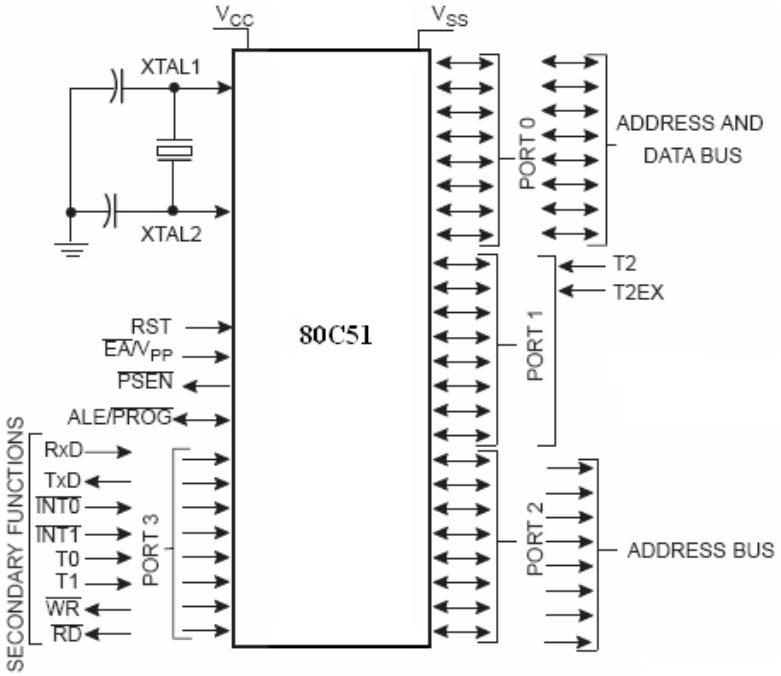


Figure 14.2 80C51 microcontroller logical symbol

- **VSS**, input pin, called ground, is the 0 V reference
- **VCC**, input pin, called power supply, represents the power supply voltage
- **P0.0–0.7**, input/output pins, form port 0, may have an 8-bit open-drain port function with Schmitt trigger inputs; can function as a data bus and less significant address bus multiplexed during access to external data and program memory using internal pull-ups
- **P1.0–P1.7**, input/output pins, form port 1, can have an 8-bit bidirectional port function with internal pull-ups and Schmitt trigger inputs; two pins can also have alternative functions
    - **T2**, input/output pin, (P1.0), represents Timer/Counter 2
    - **T2EX**, input pin, (P1.1), represents Timer/Counter 2 with capture function
- **P2.0–P2.7**, input/output pins, form port 2, may have an 8-bit bidirectional port function with internal pull-ups and Schmitt trigger inputs; as an alternative function it emits the most significant byte of the address during the access to the external program and data memory
- **P3.0–P3.7**, input/output pins, form port 3, can have an 8-bit bidirectional port function with internal pull-ups and Schmitt trigger inputs; each pin can also have an alternative function
    - **RxD**, input pin, (P3.0), represents the serial input port
    - **TxD**, output pin, (P3.1), represents the serial output port
    - **INT0**, input pin, (P3.2), represents the external interrupt 0
    - **INT1**, input pin, (P3.3), represents the external interrupt 1
    - **T0**, input pin, (P3.4), represents the external input for Timer 0
    - **T1**, input pin, (P3.5), represents the external input for Timer 1
    - **WR**, output pin, (P3.6), represents the external data memory write strobe
    - **RD**, output pin, (P3.7), represents the external data memory read strobe
- **RST**, input pin, called reset, by applying logic level 1 on this pin the microcontroller is reset

- **ALE/PROG**, input/output pin, called Address Latch Enable/Program Pulse, the ALE output pulse is used to store the least significant address byte during an access to external memory, the PROG pin is the input of the program pulse during the EPROM programming period
- **PSEN**, output pin, called Program Store Enable, represents the external program memory read strobe
- **EA\ / VPP**, input pin, called External Access Enable/Programming Supply Voltage, if EA\is externally held low, the microcontroller executes the entire code from external program memory; if EA\is externally held high, the microcontroller executes the code located at memory locations 0000H to 0FFFH from the internal ROM; VPP pin receives the programming supply voltage during EPROM programming
- **XTAL1**, input pin, called Crystal 1, represents the input to the inverting oscillator amplifier and clock generator circuit
- **XTAL2**, output pin, called Crystal 2, represents the output from the inverting oscillator amplifier

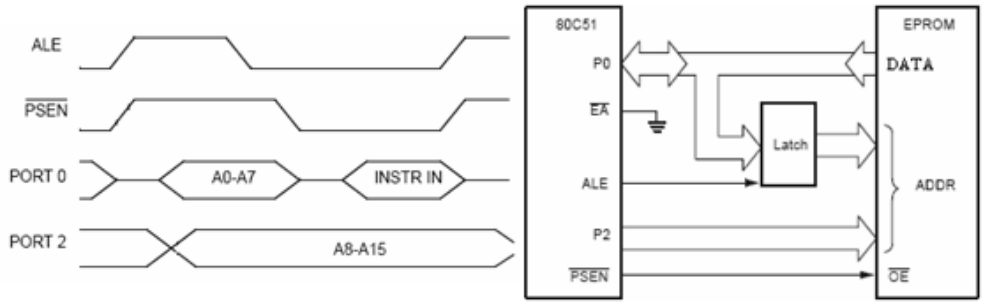


Figure 14.3 External program memory read cycle and configuration

In figure 14.3 is presented the external program memory read cycle and configuration. Address is transmitted first through P0 and P2 ports on the address bus. Because P0 port changes its function becoming data port, A0-A7 is latched when the ALE signal becomes active. PSEN\ signal becomes

active and the information in the program memory is transmitted on the data bus being received through P0 port.

In figure 14.4 is presented the external data memory read/write cycles and configuration. For the read cycle, address is transmitted first through P0 and P2 ports on the address bus. Because P0 port changes its function becoming data port, A0-A7 is latched when the ALE signal becomes active. RD\ signal becomes active and the information in the data memory is transmitted on the data bus being received through P0 port. For the write cycle, address is transmitted first through P0 and P2 ports on the address bus. Because P0 port changes its function becoming data port, A0-A7 is latched when the ALE signal becomes active. Data is transmitted through P0 port on the data bus and when WR\ signal becomes active is stored in the data memory.

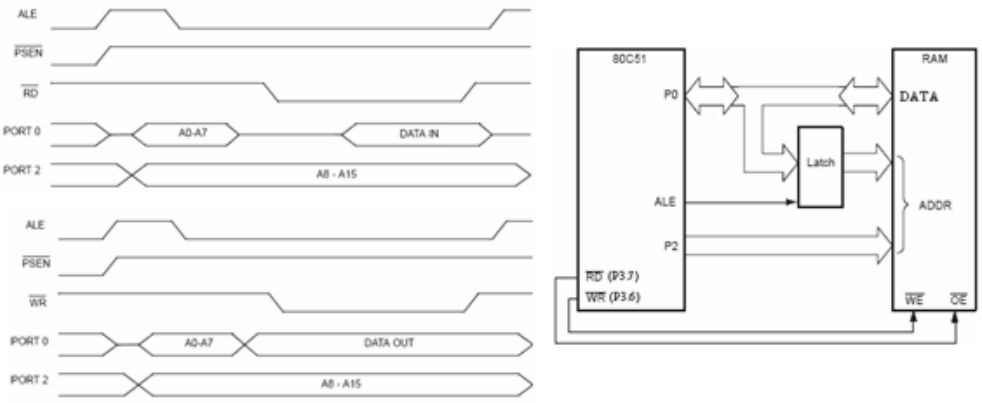


Figure 14.4 External data memory read/write cycles and configuration

3. PRACTICAL APPROACH

3.1. Theoretical aspects related to the 80C51 microcontroller family will be discussed.

3.2. It will be analyzed and discussed the microcontroller system presented

in figure 14.5, having the following blocks:

- quartz oscillator with 12MHz frequency
- reset circuit
- 8k*8 bit external program memory with the low (base) address 0000H
- output port at address 011X...Xb
- input port at address 111X...Xb, here having connected two keys
- only external program memory is used

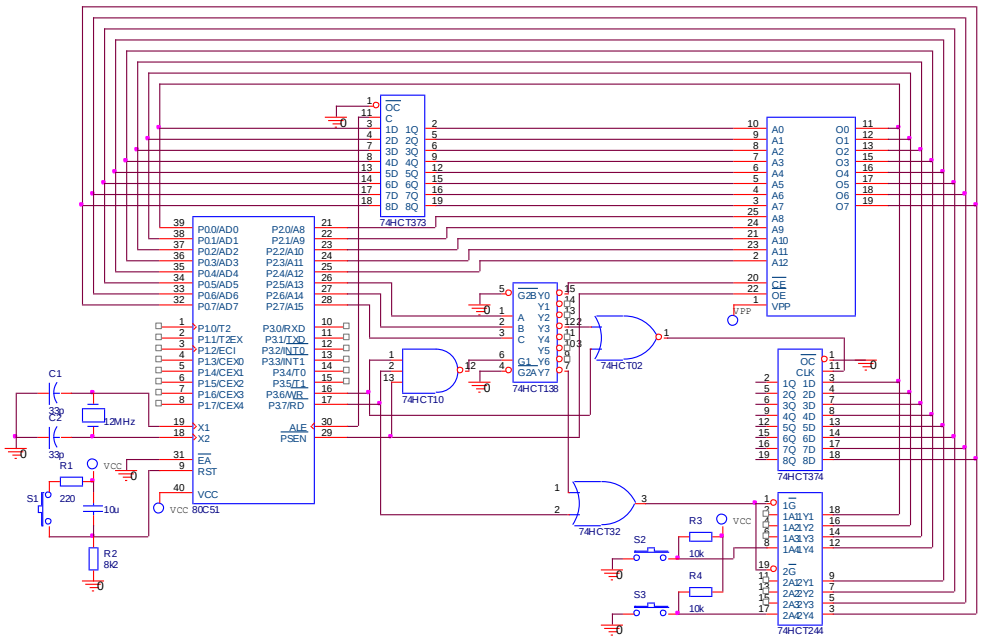


Figure 14.5 Example of 80C51 microcontroller system

3.3. Design a system based on a 80C51 microcontroller, with the following blocks:

- quartz oscillator with 12MHz frequency
- reset circuit
- 32k*8 bit external data memory with the low (base) address 8000H

- output port at address 011X...Xb having connected two 7-segments LED displays using common anode, with: V_{LED}=1,6V and I_{LED}=25mA; for transistors we consider β=100
- input port at address 010X...Xb, here having connected 8 keys; pressing any key generates the interrupt INT0\
- only internal program memory is used

4. REPORT CONTENT

4.1. Summary of the characteristics of the 80C51 family of microcontrollers.

4.2. Schematics of the 80C51 microcontroller system from point 3.3 together with the explanations related to the design and sizing of each block.

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ANNEX 1: AIM-Spice Program

1. INTRODUCTION

The AIM-Spice program is an electronic circuits simulation program for DC transfer curve analysis, AC analysis and transient analysis.

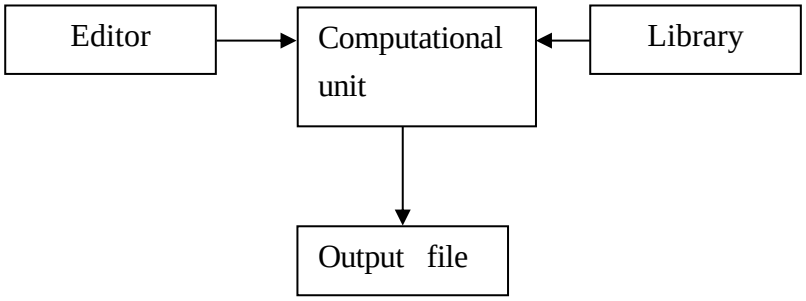

Fig.A1.1

The AIM-Spice block diagram is presented in figure A1.1. The description of the circuit is made by using an editor, each described device being modeled in the simulation program library. The computational module realizes the desired analysis generating the output file that can be visualized or printed. The program disposes of a postprocessing unit whose facilities enhances the analysis possibilities.

2.THEORETICAL CONSIDERATIONS

2.1. AIM-Spice analysis types.

2.1.1. The Operating Point computation.

Operating Point computation of a circuit is made indifferent if the command is or is not specified. This analysis computes the circuit's direct current Operating Point. There are no parameters for this analysis.

2.1.2. The DC Transfer curve analysis

This analysis type allows the determination of the analyzed electronically circuit's Operating Point, with the coils in short circuit and the capacitors in vain. DC Transfer curve it is automatically done before an AC analysis, for the purpose of linearizing the circuit.

In the DC Transfer curve analysis, one or two voltage or current sources are modified in an interval defined by the user. The Operating Point is computed for each value of the sources.

For the DC Transfer curve analysis the following parameters must be set: Source Name, Start Value, End Value and Increment Value.

Source Name is the name of an independent voltage or current source, Start Value, End Value Increment Value are the start, the end, and the increment source value, respectively. A second source may optionally be specified along with its parameters. In this case, the first source is specified in the limits for each value of the second source. This option is useful for obtaining the output characteristics of the semiconducting devices.

2.1.3. The DC Temperature Sweep Analysis

In the process of DC Temperature Sweep Analysis functioning circuit's temperature is varied in an interval defined by the user. The Operating Point of the circuit is computed for each temperature value.

The analysis has three parameters - Start Value, End Value and Increment Value – by using them it can be defined the temperature interval for which the analysis will be made. Every parameter has as its measurement unit the ºC.

2.1.4. The Transient Analysis

This analysis type computes the output variables as time functions, in an interval specified by the user. The initial conditions follows from the computation of the operating point or may be explicitly specified (.IC).

For the transient analysis, the following parameters must be set: Stepsize, Final time, Display Start Time, Maximum Stepsize and Use Initial Conditions.

The Stepsize parameter sets the computational increment of time points, Final Time is the last computed time point. The Transient Analysis always begins at time zero. If until a certain time the results are of no interest, this time will be specified through the Display Start Time parameter. The Maximum Stepsize parameter is useful when we want to limit the internal stepsize used by the AIM-Spice simulator.

When the option Use Initial Conditions (UIC) is selected, Aim-Spice will use the initial conditions defined by the user. If not, initial condition solving is done by the simulator by computing the operating point. The initial conditions may be specified in the description of the circuit by using the .IC option.

The general form for the .IC option is:

.ic v(nodename)=value v(nodename)=value ...

Example:

.ic v(11)=5 v(1)=2.3

2.1.5. The AC Analysis

In the AC analysis, the output alternating current variables are computed as frequency functions.

For the AC Analysis, the following parameters must be set: Sweep, Number of points, Start Frequency and End Frequency.

The Sweep parameter sets the input signal frequency variation. It may be DEC (decade), OCT (octave) or LIN (linear). The Number of points parameter changes together with the Sweep parameter modification. If DEC is specified, the number of points is in decade. If OCT is specified, the number of points is in octave. If LIN is specified, the number of points is the total number of points from the entire scale. The frequency scale is specified through Start frequency and End frequency parameters.

In order for the AC analysis to may be carried out, at least one independent source must be specified with an AC parameter.

If the circuit has a single ac input , is convenient to set the amplitude to one unit and the phase to zero, case when the output variable will be the transfer function of the output variable related to the input.

2.1.6. The Pole-Zero Analysis

The Pole-Zero Analysis determines the poles and the zeroes in the low signal ac transfer function. First, the operating point is computed, after this the circuit is linearized with respect to the operating point. The obtained circuit is used for determining the poles and the zeroes.

2.1.7. The Transfer Function Analysis

This analysis computes the transfer function's low signal value in direct current, the input resistance and the output resistance.

2.1.8. The Noise Analysis

The Noise Analysis computes the noise generated by the devices for a given circuit. When an input source and an output port are specified, the analysis computes the noise contributions of each device (and to each noise generator in the device) at output port voltage. Also it computes the circuit input noise, equivalent with the output noise referred to the specified input source. These computations are made for each frequency from the specified scale. The computed noise value corresponds to the circuit variable's spectral density seen as a Gaussian stationary process. After computing the spectral densities, the noise analysis integrates this values in a specified frequency scale for obtaining the total voltage/current noise (in the respective frequency scale).

The format of the parameter "Output Noise Variable" is V(OUTPUT<,REF>), where OUTPUT is the node where the total output noise is computed. The parameter "Input Source" is an independent source to which the input noise is referred. The next three parameters contains information related to the frequency, same with the ones from the AC analysis. The last parameter is an optional integer. If specified, the noise contribution at each noise generator is produced at each "Points per Summary" frequency point.

2.2. Rules for the AIM-Spice data files.

2.2.1. Data and command format in AIM-Spice.

First line is the title line and may contain any text.

The comment lines are marked by "*"in the first column, and may contain any text.

Except for the title line and the sub-circuit's definitions, the order of the lines is arbitrary.

AIM-Spice doesn't differentiate between capital letters and normal letters.

The number of blanks separating the fields of a line is not significant. Comas, parenthesis and tabs are equivalent with blanks.

A circuit line may continue on the next line by putting the sign "+" at the beginning of the line or lines where we continue.

Any component given value may be followed by a scale factor. This can be described by a letter or as a 10's multiple. The following table enumerates the scale factors in the two description forms:

F	1E-15
P	1E-12
N	1E-9
U	1E-6
MIL	25.4E-6
M	1E-3
K	1E3
MEG	1E6
G	1E9
T	1E12

2.2.2. The description of the circuit in AIM-Spice

2.2.2.1. Nodes numbering.

The name of a node may be any character sequence except for the mass node always noted with ‘’0”.

2.2.2.2. The description of the circuit’s elements.

Each element of the circuit is specified by a description instruction that contains the next fields:

- the name of the element– it must begin with a letter that specify the type of the considered circuit element;
- two or more nodes, to which the element is connected;
- a model name or the element value;
- other parameters that characterize the element.

2.3. The description of the circuit’s components

2.3.1. Resistances

General form:

RXXXXXXX N1 N2 VALUE

Examples:

R1 1 2 100

RB 1 2 10K

RBIAS 4 8 10K

N1 and N2 are the element nodes. VALUE is the resistance expressed in Ohms.

2.3.2. Coils

General form:

LYYYYYYY N+ N- VALUE <IC=Initial values>

Examples:

llink 42 69 1uh

lshunt 23 51 10u ic=15.7ma

N+ and N- are the positive and negative element nodes, respectively. VALUE is the inductance in Henry. The initial value is an optional parameter representing the initial value of the current through the coil at the moment of time zero expressed in Amperes. This value is used only when the UIC option is specified in the transient analysis.

2.3.3. Capacitors

General form:

CXXXXXXX N+ N- VALUE <IC=Initial values>

Examples:

cl 66 0 70pf

CBYP 17 23 10U IC=3V

N+ and N- are the positive and negative element nodes, respectively. VALUE is the capacitance expressed in Faradays. The initial value is an optional parameter representing the initial value of the voltage on the capacitor at zero moment of time expressed in Volts. This value is used only when the UIC option is specified in the transient analysis.

2.3.4. The semiconducting diode.

General form:

DXXXXXXX N+ N- MNAME <AREA> <OFF> <IC=VD> <TEMP=T>

Examples:

DBRIDGE 2 10 DIODE1

DCLMP 3 7 DMOD 3.0 IC=0.2

N+ and N- are the positive and negative element nodes, respectively. MNAME is the model name, AREA is the area factor, and OFF indicates an initial optional value for the DC transfer curve. If the area factor is not mentioned, it will be 1 by default. The initial optional value IC=VD is used both with UIC in the transient analysis. The initial optional value TEMP is the working temperature of the device.

The diode model:

.MODEL [model name] D <model parameters>

AIM-Spice has 2 models for the semiconducting diode: Level 1 which is the default model and Level 2. For selecting the second model LEVEL=2 will be specified in the model line.

Next, the most used parameters of the Level 1 model are presented:

Name	Parameter	Units	Default
IS	The saturating current (only for Level 1)	A	1.0e-14
RS	The ohmic resistance	W	0
N	The emission coefficient	-	1
TT	The transit time	s	0

2.3.5. Bipolar Transistor

General form:

QXXXXXXX NC NB NE <NS> MNAME <AREA> <OFF> <IC=VBE, VCE> <TEMP=T>

Example:

Q23 10 24 13 QMOD IC=0.6, 5.0

q2 5 4 0 qnd

NC, NB and NE are the collector, base and emitter nodes, respectively. NS is the substrate node. If this is not given, ground is assumed. MNAME is the model name, AREA is the area factor, and OFF indicates an

optional initial value for the element in a dc analysis. If the area factor is omitted, 1.0 is assumed. The optional initial value IC=VBE, VCE is meant to be used together with UIC in a transient analysis. See the description of the .IC statement for a better way to set transient initial conditions. The optional TEMP value is the temperature at which this device operates.

Bipolar transistor model:

.MODEL [model name] NPN <model parameters>

.MODEL [model name] PNP <model parameters>

The most used parameters of the bipolar transistor model are presented below:

Name	Parameter	Units	Implicit
IS	Saturation current	A	1e-16
BF	Amplification factor for RAN	-	100
BR	Amplification factor for RAI	-	1
RE	Emitter resistance	W	0
RC	Collector resistance	W	0
TF	Falling time	S	0
TR	Rising time	S	0

2.3.6. MOS Transistor

General form:

MXXXXXXX ND NG NS NB MNAME <L=VALUE> <W=VALUE> <AD=VALUE>

<AS=VALUE><PD=VALUE><PS=VALUE><NRD=VALUE>

+<NRS=VALUE><OFF><IC=VDS, VGS, VBS><TEMP=T>

Example:

M1 24 2 0 20 TYPE1

m15 15 15 12 32 m w=12.7u l=207.8u

M1 2 9 3 0 MOD1 L=10U W=5U AD=100P AS=100P PD=40U PS=40U

ND, NG, NS and NB are the drain, gate, source and bulk (substrate) nodes, respectively. MNAME is the model name; L and W are the channel length and width in meters, respectively. AD and AS are the drain and source diffusion areas in square meters. PD and PS are the perimeters of the drain and source diffusion areas. NRD and NRS are the relative resistivities of the drain and source in number of squares, respectively. OFF indicates an optional initial value for the element in a dc analysis. If the area factor is omitted, 1 is assumed. The optional initial value IC=VDS, VGS, VBS is meant to be used together with UIC in a transient analysis. The optional TEMP value is the temperature at which this device operates. It overrides the temperature specified in the option value.

MOS Transistor Model:

.MODEL [model name] NMOS <model parameters>

.MODEL [model name] PMOS <model parameters>

AIM-Spice supports 17 MOS models. The parameter LEVEL selects which model to use. The default is LEVEL=1.

2.4. Sub-circuits

2.4.1. Sub-circuits definition

When a circuit contains many identical blocks or subcircuits, it is convenient to be able to write a block once and then reference it when needed. Digital circuits, for example, are described easier in this way.

A subcircuit is defined in terms of a block of lines that start with the line .SUBCKT and ends with the line .ENDS. Between these lines, there are one or more devices, models, calls to other subcircuits, and even new subcircuit definitions. When a subcircuit has been defined, it can be referenced as a device with a name that starts with the letter 'X'.

Nodes can be defined as terminals for a subcircuit, making it possible to connect the subcircuit to the rest of the circuit. Node names used in subcircuit definitions are local names, and they will not come in conflict with global node names in the main circuit.

General form:

.subckt [subcircuit name] n1 n2 n3 … <PARAM:PAR=VAL…>

Example:

```
.subckt  opamp 1  2  3  4  5
```

A subcircuit definition starts with the .subckt statement. subcircuit name is the name of the subcircuit used when referencing the subcircuit. n1, n2 ... are external nodes, excluding "0" which is the ground node. PARAM is a keyword indicating parameter allocation within the subcircuit definition. PAR=VAL specifies that the parameter PAR is assigned the value VAL inside the subcircuit, unless another value is assigned to the parameter when the subcircuit is instantiated.

The group of elements that follows directly after the .subckt statement defines the topology of the subcircuit. The definition must end with the .ends statement. Control statements are not allowed in a subcircuit definition. A subcircuit definition can contain other subcircuit definitions, device models, and call to other subcircuits. Note that device models and subcircuit definitions within a subcircuit definition are local to that subcircuit and are not available outside. Nodes used in a subcircuit are also local, except "0" (ground) which is always global.

Example:

```
.SUBCKT INV 1 2 3

M1 3 2 1 1  MOSP   W=24U   L=1.4U

M2 3 2 0 0 MOSN W=12U L=1.0U

.ENDS
```

This example describes a CMOS inverter defined as a subcircuit.

2.4.2. Subcircuits call

General form:

XYYYYYYY N1 <N2…>SUBNAME<PAR=VAL><PAR={EXPRESION}>

Example:

X1 2 4 17 3 1 MULTI

A line that starts with an 'X' is used to instantiate a subcircuit that has been defined using the .subckt statement.

N1, N2 … are the names of the nodes, of the principal circuit, at which the subcircuit will be connected SUBNAME is the name of the subcircuit being instantiated, as specified by the SUBCKT. <PAR=VAL> and <PAR={EXPRESSION}> specifies that the parameter PAR is assigned a value inside the subcircuit. This parameter assignment takes precedence over any parameter assignments occurring in the .subckt statement.

2.5. Independent voltage supply

General form:

VXXXXXXX N+ N- <<DC> DC/TRAN VALUE><AC<ACMAG <ACPHASE>>> + <DISTOF1 <F1MAG<F1PHASE>>> <DISTOF2 <F2MAG <F2PHASE>>>

Example:

Vin 21 0 pulse (0 5 1ns 5ns 10us)

```
Vcc 10  0  dc  6
Vmeas 12  9
```

N+ and N- are the positive and negative nodes, respectively. Note that the voltage sources need not to be grounded. If you insert a voltage source with a zero value, it can be used as an Ampere meter.

DC/TRAN is the source value during a dc or a transient analysis. The value can be omitted if it is zero for both the DC and transient analysis. If the source is time invariant, its value can be prefixed with DC.

ACMAG is amplitude value and ACPHASE is the phase value of the source during an ac analysis. If ACMAG is omitted after the keyword AC, 1 is assumed. If ACPHASE is omitted, 0 is assumed.

DISTOF1 and DISTOF2 are the keywords that specify that the independent source has distortion inputs at the frequencies F1 and F2 respectively (see the description of the distortion analysis parameters). The keywords may be followed by an optional magnitude and phase. The default values of the magnitude and phase are 1.0 and 0.0 respectively.

All independent sources can be assigned time varying values during a transient analysis. If a source is assigned a time varying value, the value at t=0 is used during a dc analysis. There are 5 predefined functions for time varying sources: pulse, exponent, sinusoidal, piece-wise linear and single frequency FM. If parameters are omitted, the default values shown in the tables below will be assumed. DT and T2 are the increment time and final time in a transient analysis, respectively.

Pulse

General form:

PULSE (V1 V2 TD TR TF PW PER)

Parameter	Implicit Value	Unit
V1 (initial value)	-	V
V2 (pulsed value)	-	V
TD (delay time)	0.0	s
TR (rise time)	DT	s
TF (fall time)	DT	s
PW (pulse width)	T2	s
PER (period)	T2	

Example:

VIN 3 0 PULSE (1 5 1S 0.1S 0.4S 0.5S 2S)

SINUS

General form:

SIN (V0 VA FREQ TD THETA)

Parameter	Implicit value	Unit
V0 (offset)	-	V
VA (amplitude)	-	V
FREQ (frequency)	1/T2	Hz

TD (delay)	0.0	s
THETA (damping factor)	0.0	1/s

Example:

VIN 3 0 sin (2 2 5 1s 1)

EXPONENT

General form:

EXP (V1 V2 TD1 TAU1 TD2 TAU2)

Parameter	Implicit value	Unit
V1 (initial value)	-	V
VA (pulsed value)	-	V
TD1(rise delay time)	0.0	s
TAU1(rise time constant)	DT	s
TD2 (delay fall time)	TD1+DT	s
TAU2 (fall time constant)	DT	s

Example:

VIN 3 0 EXP (1 5 1S 0.2S 2S 0.5S)

Piece-wise Linear

General form:

PWL (T1 V1<T2 V2 T3 V3 T4 V4 T5 V5 …>)

Parameters and default values:

Every pair of values (Ti, Vi) specifies that the value of the source is Vi at Ti. The value of the source between these values is calculated using a linear interpolation

Example:

VCLOCK 7 5 PWL (0 0 1 0 1.2 4 1.6 2.0 5.0 3.0 1.0)

Single frequency FM

General form:

SFFM (V0 VA FC MDI FS)

Parameter	Implicit value	Unit
V0 (offset)	-	V
VA (amplitude)	-	V
FC (carrier frequency)	1/T2	Hz

MDI (modulation index)	-	-
FS (signal frequency)	1/T2	Hz

Example:

VIN 12 0 SFFM (2 1 2 5 0.2)

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