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ELECTRONIC DEVICES

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To our dear students

Foreword

As the fascinating, yet not simple, world of electronics may seem intimidating, we aim to provide our first-year students with the support they need. Over decades of teaching between us, we noticed that a successful learning experience is the result of accumulating knowledge that was delivered in multiple ways. The theoretical notions discussed during lectures are better understood when applied into examples and validated by practical experiments. This book is designed to accompany the course slides and guide the young engineers-to-be throughout their journey into not only studying, but also understanding, how the most used electronic devices work.

Each chapter follows the same pattern, which ensures a unitary structure of the entire material. Theoretical notions are first presented, then used in solved examples. The book is meant to minimize the temptation of memorizing circuits equations, such a trap for most students. We believe that any knowledge is best learned when applied, hence the proposed problems at the end of each chapter.

Chapter 1 – Fundamentals is an overview of fundamental concepts that will be used in subsequent chapters. Students can always revisit this section, for a quick memory refresh.

Chapter 2 is dedicated to diodes, semiconductor devices that are analysed starting with their physical structure and operating regions, followed by the exponential model, and the constant voltage drop model. The most common diode circuits are presented, along with relevant examples. Zener diodes are also discussed, with their behaviour, operating regions, and common applications. The chapter closes on LEDs and photodiodes.

In Chapter 3 – Electronic Amplifiers, the amplifier is seen as a functional block, and its parameters and modelling are discussed. Next, Chapter 4 puts the operational amplifier as an integrated circuit under the spotlight, focusing on its terminal behaviour, without any details regarding its internal structure. Its use in typical circuits and applications is analysed: simple and positive feedback comparators, and amplifiers.

The third and last electronic device approached in this book is the transistor. Chapter 5 begins with presenting general concepts, valid for all transistor types, which are then customized for the BJT and the MOSFET. The highlight is on identifying the operating regions and biasing the transistor into the desired region.

By the end of the book, the avid reader who follows all the solved examples and doesn't quit when faced with the proposed problems will be able to:

- know and understand the basic concepts regarding the operation and use of electronic devices
- use electronic devices in simple electronic circuits
- analyse, design and (re)size simple electronic circuits

We believe that for things to be truly great, there must be a little magic involved. It is our hope that this book delivers the sparkle of magic needed to transform students into passionate engineers.

Cluj – Napoca, May 2023

The authors

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Chapter 1

FUNDAMENTALS

In this chapter, you will learn:

- mathematical expressions and graphical representations of electrical signals
- symbols and notations for ac and dc signal sources
- relationships and theorems for analysing electronic circuits
- time-domain and frequency-domain behaviour of passive electronic components.

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1.1 Electrical signals. Signal sources. Notations.

Signals are variables that contain information, regardless of its nature: sound, image, temperature, pressure, speed, etc. In electronics, the focus is on *electrical signals*:

- *electrical voltage* or *voltage*: notation *v* or *V,* unit of measurement Volt [V], and submultiples: mV (1 mV = 10^{-3} V), µV (1 µV = 10^{-6} V)
- *electrical current* or *current*: notation *i* or *I,* unit of measurement Ampere [A], and submultiples: mA (1 mA = 10^{-3} A), µA (1 µA = 10^{-6} A)

Based on the way they vary with respect to time, electrical signals are classified into:

- *continuous signals*: signals that are constant over time; these are referred to as *dc signals* (direct current)
- *time-varying signals*: signals that vary over time; these are referred to as *ac signals* (alternating current).

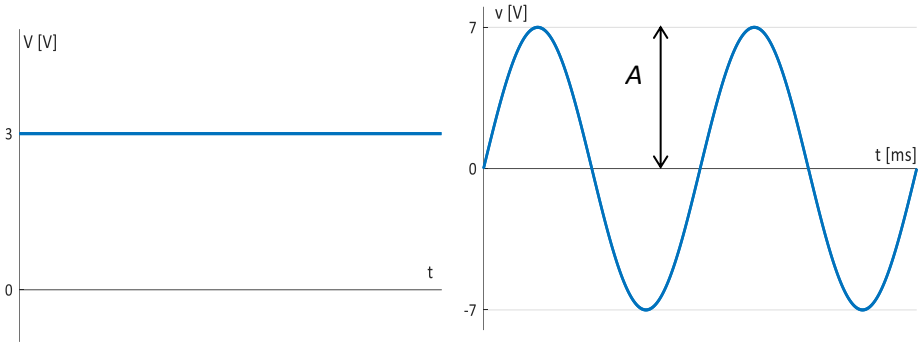
To illustrate this concept, Fig.1.1 shows a dc voltage, V = 3 V (a), and a sinusoidal voltage (sine wave), $v = 7\sin\omega t$ [V] (b).

The parameters of the sinusoidal signal in Fig.1.1. b) are:

- amplitude - A = 7 V
- peak-to-peak value - V_{pp} = 14 V, computed as the difference between the maximum and the minimum value of the signal
- RMS (root mean square) of effective value

$$V_{rms} = \frac{A}{\sqrt{2}} = 4.96 \text{ V}$$

- period - T = 2 ms, or frequency f = 0.5 kHZ
- average value or dc component on a time interval (for periodic signals, the average value is computed on a period). Since the positive half-cycle of the sinusoidal wave is equal to the negative one, the average value of the sinusoidal wave is zero. We say that *the sine wave is centred on zero volts* or *has a dc component or offset of zero volts*.
- instantaneous value – the value of the signal at a certain time. For example, at $t = T/4$, the instantaneous value is +7 V.



a) b)

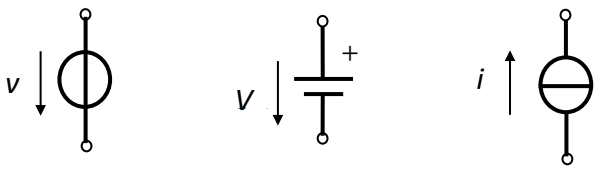
Fig.1.1. Waveforms a) dc voltage; b) sinusoidal voltage.

Sinusoidal signals are most used. Home appliances (washing machines, refrigerators, air conditioners, dishwashers, water heaters, etc.) and electronic devices (computers, laptops, TV sets, mobile phones, etc.) are supplied with a sinusoidal voltage of 230 V effective value, 325 V amplitude and 50 Hz frequency (EU standard). In the United States, the effective value of the power line voltage is 117 V, with a frequency of 60 Hz.

Note: When measuring a sinusoidal voltage using a voltmeter, the indicated value is the RMS or effective value of the voltage.

Other types of time-varying signals are triangular, rectangular (square), sawtooth, positive/negative pulse, step signals, etc.

The symbols used for electrical signal sources are shown in Fig.1.3. The „+" sign is occasionally added, to indicate the positive terminal:



a) b) c)

Fig.1.3. Symbols for signal sources
a) voltage source; b) dc voltage source; c) current source.

Example

The plot for $v_S(t) = 6 + 2\sin\omega t$ [V] is given in Fig.1.2. The dc component (average value) is 6 V (dotted line), and the ac (variable) component is $2\sin\omega t$ [V]. The plot starts at 6 V, and the extreme values are 6 ± 2 V.
The peak-to-peak value is 4 V.

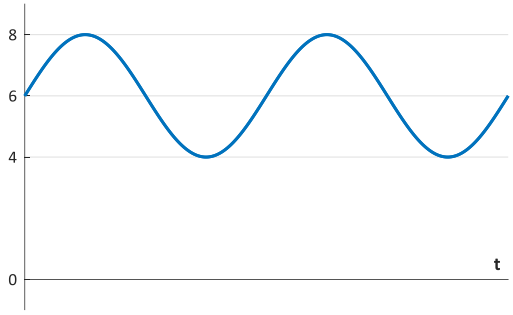


Fig.1.2. Graphical representation of $v_S(t) = 6 + 2\sin\omega t$ [V]

To correctly identify the types of signals, a convention is employed (Fig.1.4):

- continuous (dc) signal only - uppercase variable and uppercase subscript V_S, I_S
- time-varying (ac) signal only - lowercase variable and lowercase subscript v_s, i_s
- total instantaneous signal (continuous and time-varying signal) - lowercase variable and uppercase subscript v_S, i_S.

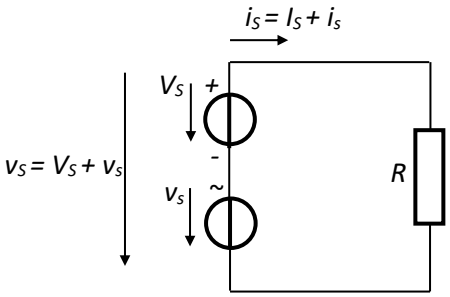


Fig.1.4. Signal notations

Problems

Plot the following signals:

a. $v_S(t) = 5\sin\omega t$ [V]
b. $v_S(t) = 1 + 4\sin\omega t$ [V]
c. $v_S(t) = -2 + 3\sin\omega t$ [V]
d. $v_S(t) = 2 - 3\sin\omega t$ [V]

1.2 Relations and theorems for electrical circuits

1.2.1 Ohm's law

Ohm's law is named after German physicist Georg Ohm, who analysed the measured values of voltages and currents in simple electrical circuits and published his work in 1827. Ohm's law states that the voltage drop across a resistor and the current through that resistor are proportional. The resistance value, *R,* is the proportionality factor.

$$V = R \cdot I$$

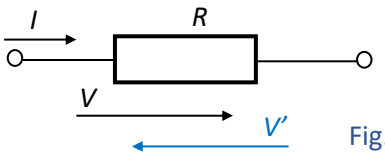


Fig.1.5. Ohm's law illustration

If the arbitrary chosen directions for voltage and current are opposite, a minus sign appears when writing Ohm's law (see Fig.1.5):

$$V' = - R \cdot I$$

1.2.2 Kirchhoff's theorems

Gustav Robert Kirchhoff first formulated the circuits laws in 1845, while still a student. These theorems are used for the analysis of electrical circuits.

- Kirchhoff's first theorem or *Kirchhoff's current law* (KCL):

"The algebraic sum of all currents in a network of conductors meeting at a point (or node) is zero."

Currents entering the node are added to the sum, while currents that exit the node are subtracted. To illustrate KCL, for node *N* in Fig.1.6, currents I_1 and I_2 enter the node, and current I_3 exits the node. Thus, KCL for node *N* is expressed as:

$$I_1 + I_2 - I_3 = 0$$

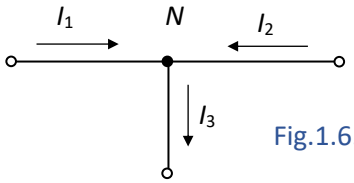


Fig.1.6. Illustration of KCL

Note: KCL can also be interpreted as: in any circuit node, there isn't any current consumption, or current generation. All the current that goes into the node must also exit the node.

- *Kirchhoff's second theorem* or *Kirchhoff's voltage law* (*KVL*):

"The algebraic sum of all voltages in a closed circuit is zero."

To apply this theorem, an arbitrary direction (clockwise or counterclockwise) must be chosen. The voltages that have the same direction as the chosen one will be added, while the ones in the opposite direction will be subtracted. For a voltage source, the voltage across its terminals is considered, and not the electromotive voltage.

To illustrate KVL, Fig.1.7. a) shows a circuit with chosen clockwise direction for the loop. KVL is expressed as:

$$- V_1 + V_{R1} + V_2 - V_{R2} = 0$$

This equation can be further detailed by using Ohm's law to express the voltage drops across

resistors:

$$- V_1 + R_1 \cdot I + V_2 - R_2 \cdot I = 0$$

When choosing the counterclockwise direction (Fig.1.7. b), KVL is:

$$V_1 - R_1 \cdot I - V_2 + R_2 \cdot I = 0$$

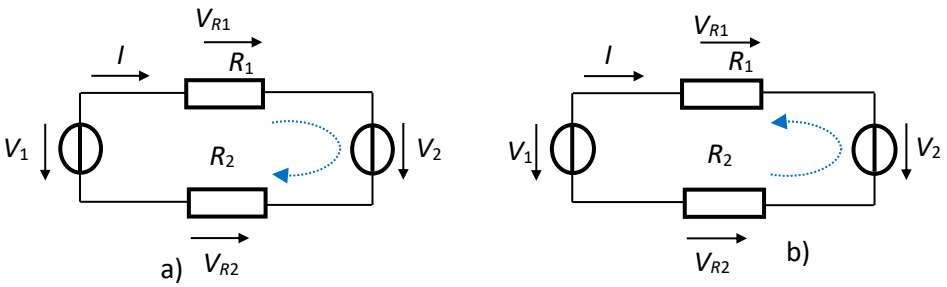


Fig.1.7. Illustration of KVL
a) clockwise; b) counterclockwise.

1.2.3 Resistor connections

- The series connection

Two or more resistors are connected in series if the same current flows through all of them (Fig.1.8).

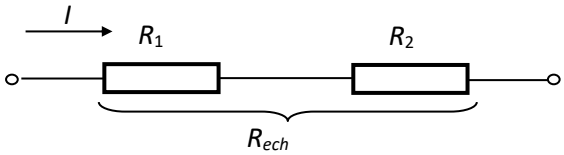


Fig.1.8. Series connection of two resistors

$$R_{ech} = R_1 + R_2$$

The equivalent resistance of two or more series resistors is always greater than any of the individual resistances.

- The parallel connection

Two or more resistors are connected in parallel if the same voltage drop appears across each resistor (Fig.1.9).

$$R_{ech} = \frac{R_1 \cdot R_2}{R_1 + R_2}$$

The equivalent resistance of two or more resistors in parallel is always smaller than any of the individual resistances. For *n* resistors in parallel, the equivalent resistance is computed as:

$$\frac{1}{R_{ech}} = \sum_{i=1}^{n} \frac{1}{R_i}$$

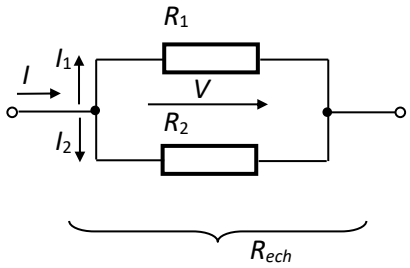


Fig.1.9. Parallel connection of two resistors

Tricks:

→ The equivalent resistance of a high value resistor connected in series (parallel) with a low value resistor can be considered equal to the high (low) resistance.

Example: For R_1 = 100 kΩ and R_2 = 1 kΩ:

Series connection: $R_{series} \approx 100$ kΩ

Parallel connection: $R_{parallel} \approx 1$ kΩ.

→ To compute the equivalent resistance of 10 kΩ in parallel with 20 kΩ, the 10 kΩ resistor can be seen as two 20 kΩ resistors in parallel, which results in having to compute the parallel equivalent of three 20 kΩ resistors (20 kΩ/3 = 6.66 kΩ).

These tricks speed up the computation part of the circuit analysis. It is recommended to avoid computing the values of circuit components using too many decimal places (high precision), since:

1. the values of electronic components have a finite precision (typical tolerance for resistors is 5% or 1%)
2. a carefully designed electronic circuit is almost always immune to the variations of nominal, precise values of electronic components.

1.2.4 Resistive dividers

- The voltage divider

A voltage divider delivers a predictable fraction of the input voltage at the output. Any real electronic circuit contains voltage dividers, as they are one of the most widespread electronic circuit parts.

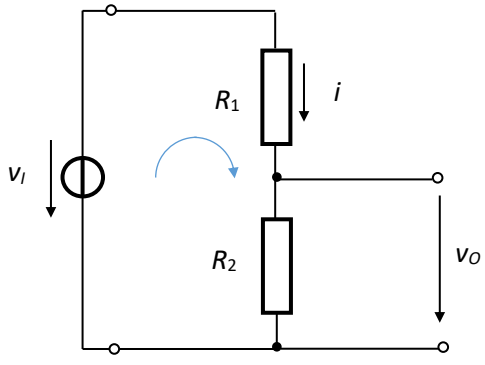


Fig.1.10. Voltage divider

The equations for the circuit in Fig.1.10 are:

$$i = \frac{v_I}{R_1 + R_2}$$

$$v_O = i \cdot R_2 = \frac{R_2}{R_1 + R_2} \cdot v_I$$

The voltage drop across a resistor is proportional with its value and inversely proportional with the sum of all resistances in the circuit. For a constant input voltage, if R_2 increases, the output voltage, which is the voltage drop across R_2, also increases.

Example

Size the voltage divider in Fig.1.10, so that for an input voltage V_I = 15 V, the output voltage is V_O = 5 V.

Solution:

Using the equation for V_O, we solve for R_1 and R_2:

$$V_O = i \cdot R_2 = \frac{R_2}{R_1 + R_2} \cdot V_I$$

$$\frac{R_2}{R_1 + R_2} = \frac{V_O}{V_I} = \frac{1}{3}$$

$$R_1 = 2 \cdot R_2$$

Any pair of values that satisfy the relation can be chosen for R_1 and R_2. For example, R_1 = 10 kΩ and R_2 = 5 kΩ.

To obtain an adjustable voltage divider, all we need is an adjustable resistor, called *potentiometer* (Fig.1.11). The potentiometer allows the adjustment of the division factor between the input and output voltages. This factor varies between 0 and 1. The output voltage is measured across a fraction of the potentiometer ($k \cdot P$).

$$v_O = \frac{k \cdot P}{P} v_I = k \cdot v_I$$

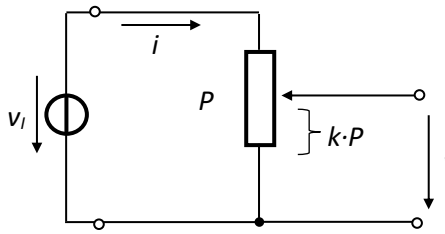


Fig.1.11. Adjustable voltage divider

The most common application of this simple resistive divider is volume control for audio amplifiers.

The division factor between the input and output voltages can be modified by placing one or two resistors, in series with the potentiometer.

Example

Design and size an adjustable voltage divider, so that for an input voltage V_I = 12 V, the output voltage is adjustable, $V_O \in$[5 V; 12 V].

Solution:

Since the output voltage needs to be adjustable, the circuit must contain a potentiometer. For the circuit in Fig.1.1, the range of values for V_O is [0; V_I], that is [0; 12] [V].

The correct solution is given in Fig.1.12, where an additional resistor R is added, in series with potentiometer P.
The output voltage V_O becomes:

$$V_O = \frac{k \cdot P + R}{P + R} \cdot V_I$$

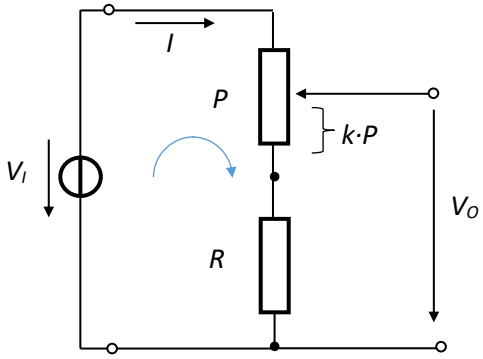


Fig.1.12. Final circuit for the adjustable voltage divider with R and P

Based on the specified extreme values for V_O:

$$\text{for } k = 0 \Rightarrow V_{Omin} = \frac{R}{P + R} \cdot V_I = 5 \text{ V}$$

$$\text{for } k = 1 \Rightarrow V_{Omax} = \frac{P + R}{P + R} \cdot V_I = V_I = 12 \text{ V}$$

Knowing that $V_I = 12$ V, the equation for R and P becomes

$$\frac{R}{P + R} = \frac{5}{12}$$

The obvious solution is to choose $P = 5$ kΩ, $R = 7$ kΩ. Any other pair of values that satisfies the above equation is considered a viable solution. The values of R and P are usually given in kΩ.

Problems

1. Design and size a voltage divider for $V_I = 20$ V that outputs an adjustable $V_O \in [5 \text{ V}; 12 \text{ V}]$.
Hint: Since none of the extreme values of V_O are equal to V_I, the solution is to add another resistor to the schematic in Fig.1.12, above P.

2. Design and size a voltage divider for $V_I = 20$ V that outputs an adjustable $V_O \in [0 \text{ V}; 12 \text{ V}]$.
Hint: The maximum value of V_O is different from V_I, and the minimum value is 0 V, which is the exact opposite to the V_O for the schematic in Fig.1.12. The solution is to switch the position of the two components (potentiometer P will be connected to ground).

3. Design and size a voltage divider for $V_I = -14$ V that outputs an adjustable $V_O \in [-2 \text{ V}; -10 \text{ V}]$.

- The current divider

The equations for the circuit in Fig.1.13 are:

$$KCL: \quad i = i_1 + i_2$$
$$KVL: \quad R_1 \cdot i_1 - R_2 \cdot i_2 = 0$$

The solutions for the two linear equations system are:

$$i_1 = \frac{R_2}{R_1 + R_2} \cdot i; \quad i_2 = \frac{R_1}{R_1 + R_2} \cdot i$$

Assuming i is the input current, any of i_1 and i_2 can be seen as the output current. If i is constant, an increase in R_2 will decrease i_2, and consequently increase i_1.

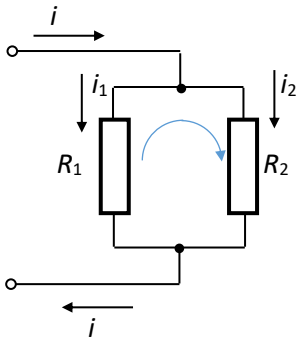


Fig.1.13. Current divider

1.2.5 The superposition method

Aside from Kirchhoff's theorems, which are valid for any circuit (linear or nonlinear), there are other methods that can be employed when analysing linear circuits.

An electronic circuit is said to be linear if the response of the circuit to a linear combination of input signals equals the linear combination of responses due to each signal, applied separately. In other words, if $f(x_1)$ and $f(x_2)$ are the responses of the circuit to input signals x_1 and respectively x_2, then the response of the circuit to input signal $(x_1 + x_2)$ is:

$$f(x_1 + x_2) = f(x_1) + f(x_2)$$

When analysing linear circuits, the *superposition method* if often employed. Using the superposition method, the response of a linear circuit with multiple input sources (voltage, current) is given by the sum of the individual responses of the circuit to each input source, when all other sources are assumed passive (reduced to zero).

Assuming a source passive means setting it to zero, that is replacing it with its internal resistance, as follows:

- a passive voltage source is equivalent to a short-circuit: the voltage at its terminals is 0 V, and the internal resistance is 0 Ω – Fig.1.14. a)
- a passive current source is equivalent to an open circuit: the current through the source is 0 A, and the internal resistance is ∞ - Fig.1.14. b).

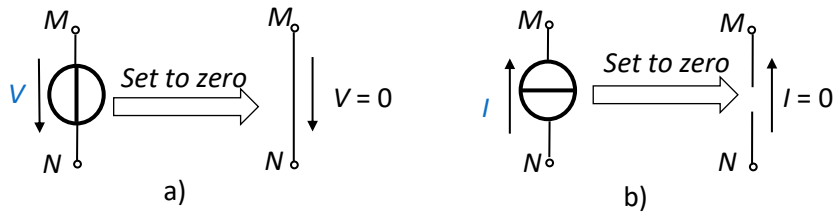


Fig.1.14. Sources set to zero (passive)
a) voltage source; b) current source.

Example

Compute the output voltage V_O for the schematic in Fig.1.15.

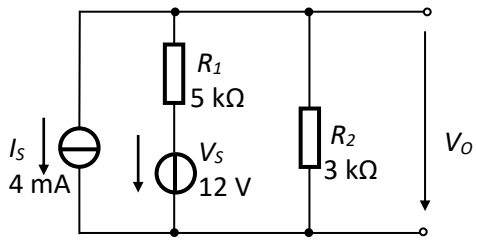


Fig.1.15. Superposition method - illustration

Solution:

Using the superposition method, the partial effects of the two input sources upon the output voltage are first determined. The result is the sum between the two partial output voltages.

Since the circuit contains two input sources, there are two equivalent circuits to work on, in order to determine the partial effects of the inputs. By assuming the input sources passive, the current source I_S becomes open circuit (Fig.1.16. a), whereas the voltage source V_S becomes short-circuit (Fig.1.16. b).

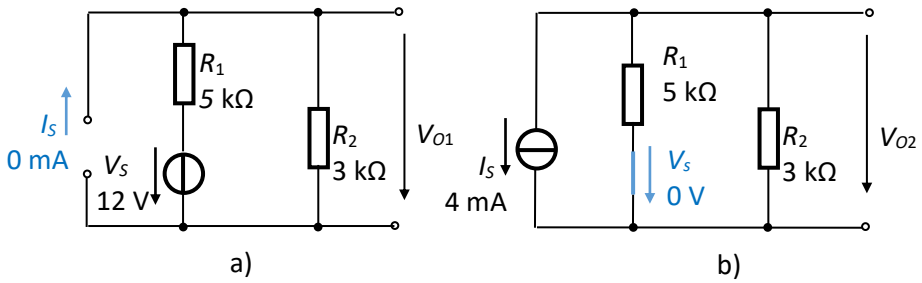


Fig.1.16. Equivalent circuits for applying the superposition method
a) passive current source; b) passive voltage source.

The effect of the voltage source V_S upon the output voltage is computed using the voltage divider for the equivalent circuit in Fig.1.16. a). The two resistors are in series (same current through both). The partial output voltage V_{O1} is:

$$V_{O1} = \frac{R_2}{R_1 + R_2} \cdot V_S = \frac{3}{5 + 3} \cdot 12 = 4.5 \text{ V}$$

The effect of the current source I_S upon the output voltage is computed using Ohm's law in the equivalent circuit in Fig.1.16. b). Resistors R_1 and R_2 are connected in parallel, and the current through the circuit is given by the current source. The partial output voltage V_{O2} is opposite to the current I_S:

$$V_{O2} = - \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot I_S = - \frac{5 \cdot 3 \cdot 10^6}{(5 + 3) \cdot 10^3} \cdot 4 \cdot 10^{-3} = - 7.5 \text{ V}$$

The total output voltage is the sum of the two partial output voltages:

$$V_O = V_{O1} + V_{O2} = 4.5 + (-7.5) = -3 \text{ V}$$

1.2.6 Thevenin's theorem

According to *Thevenin's theorem*, any network of resistors and source can be replaced with an equivalent circuit, containing an equivalent voltage source V_{Th} in series with an equivalent resistor R_{Th}. The theorem is also known as *the equivalent voltage generator theorem*, as it equivalates the given circuit with a real voltage source.

The equivalent voltage source V_{Th} is the open-circuit output voltage of the given circuit (no load connected at the output), while R_{Th} is the equivalent resistance of the given circuit, with all sources set to zero.

Example

By applying Thevenin's theorem for the circuit in Fig.1.17. a), the equivalent real voltage source in Fig.1.17. b) is obtained.

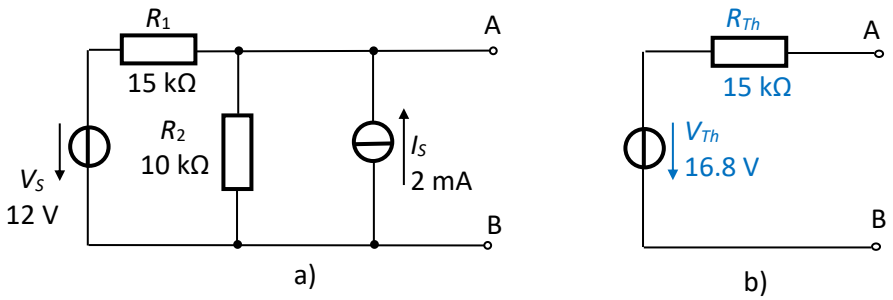


Fig.1.17. Illustration of Thevenin's theorem
a) initial circuit; b) equivalent real voltage source.

To determine V_{Th}, measured between points A and B in Fig.1.17. b), the superposition method is used:

$$V_{Th} = \frac{R_2}{R_1 + R_2} \cdot V_S + \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot I_S = \frac{10}{15 + 10} \cdot 12 + \frac{15 \cdot 10}{15 + 10} \cdot 2 = 4.8 + 12 = 16.8 \text{ V}$$

To determine R_{Th}, the sources are set to zero (Fig.1.18).

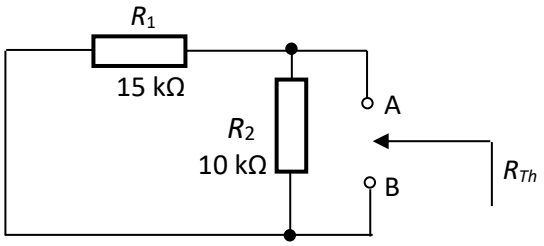


Fig.1.18. Equivalent circuit for computing R_{Th}

The equivalent resistance is:

$$R_{Th} = \frac{R_1 \cdot R_2}{R_1 + R_2} = \frac{15 \cdot 10}{15 + 10} = 6 \text{ k}\Omega$$

R_{Th} represents the resistance seen between the two terminals of the circuit, known as *the output resistance* or *the internal resistance* (of the equivalent voltage source).

Its value can also be determined by using the short-circuit current at gate AB (Fig.1.17. a).

$$R_{Th} = \frac{v_{Th}}{i_{sc}}$$

Note: There is another theorem that can be used to analyse linear circuits – *Norton's theorem*, or *the theorem of the equivalent current generator*.

1.2.7 Millman's theorem

Millman's theorem (or *the parallel generator theorem*) is used to compute the potential in a current node, based on the conductance of the parallel-connected branches, each branch with its own voltage source. The same reference point (usually ground) is assumed for all branches.

To illustrate Millman's theorem, for the circuit in Fig.1.19, the voltage in node *N* is computed as:

$$V = \frac{\sum_{k=1}^{n} V_k \cdot G_k}{\sum_{k=1}^{n} G_k} = \frac{\sum_{k=1}^{n} V_k \cdot \frac{1}{R_k}}{\sum_{k=1}^{n} \frac{1}{R_k}}$$

where *G* is the conductance, measured in *S* (siemens), $G = 1/R$.

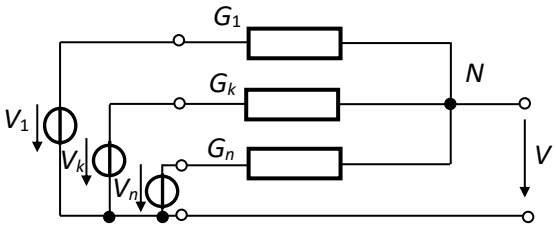


Fig.1.19. Illustration of Millman's theorem

Example

For the circuit in Fig.1.20, compute the potential V_N in node *N*, assuming *M* is the reference node. By applying Millman's theorem, V_N is computed as:

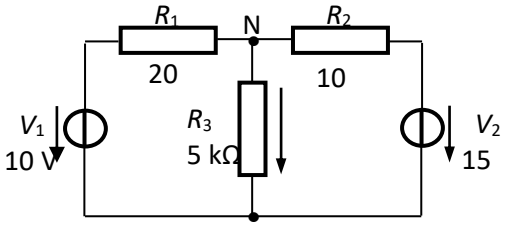


Fig.1.20. Illustration of Millman's theorem - example

$$V_N = \frac{V_1 \cdot G_1 + V_2 \cdot G_2 + 0 \cdot G_3}{G_1 + G_2 + G_3} = \frac{V_1 \cdot \frac{1}{R_1} + V_2 \cdot \frac{1}{R_2} + 0 \cdot \frac{1}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}} = \frac{\frac{10}{20} + \frac{15}{10}}{\frac{1}{20} + \frac{1}{10} + \frac{1}{5}} = 5.71 \text{ V}$$

Note: The circuit in Fig.1.20 can also be solved using the superposition method, voltage divider, Ohm's law, KVL and KCL.

1.2.8 Power

The power P for an electronic circuit (Fig.1.21) is the product between the voltage drop across the circuit (V) and the current through the circuit (I):

$$P = I \cdot V \ \text{[W]}$$

The unit of measurement for power is W (Watt), with its submultiple 1 mW = 10^{-3} W and multiples 1 kW = 10^3 W, 1 MW = 10^6 W, 1 GW = 10^9 W.

With the directions from Fig.1.21, where the voltage and current have the same direction, if the power $P > 0$, the power is *consumed* or *dissipated* (the circuit consumes power). Otherwise, if $P < 0$, the power is *generated* (the circuit generates power).

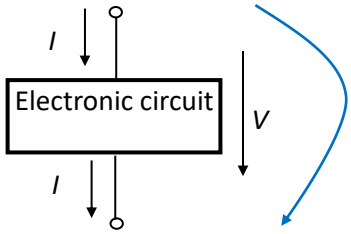


Fig.1.21. Current, voltage, power for an electronic circuit

Example

For the circuit in Fig.1.22, compute the currents I, I', the power generated by the source, P_S, and the power dissipated by the resistor, P_R.

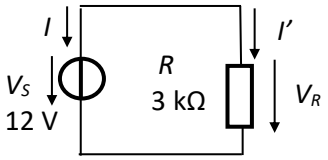


Fig.1.22. Illustration for computing the power

$$I = -\frac{V_S}{R} = -3 \text{ mA}$$
$$I' = -I = 3 \text{ mA}$$

The power generated by the source is $P_S = V_S \cdot I = 12 \text{ V} \cdot (-3 \text{ mA}) = -36$ mW. The power dissipated or consumed by the resistor is $P_R = V_R \cdot I' = 12 \text{ V} \cdot 3 \text{ mA} = 36$ mW.

Note: The same direction for the voltage and the current was considered (the receptors convention). If the voltage and the current have opposite directions (the generators convention), the interpretation of the powers is as follows: if $P > 0$, the power is *generated*, if $P < 0$, the power is consumed.

Power conservation: in an electronic circuit, the power is conserved, meaning that the generated power is equal to the dissipated power, in absolute value.

Using Ohm's law, the power dissipated by the resistors becomes:

$$P = I^2 \cdot R = \frac{V^2}{R}$$

1.3 The capacitor

The symbols for capacitors are depicted in Fig.1.23. The unit of measurement is Farad (F), with its 1 µF = 10^{-6} F, 1 nF = 10^{-9}F, 1 pF = 10^{-12} F.

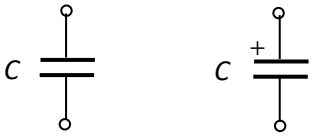


Fig.1.23. Symbols for capacitors

1.3.1 Current-voltage relation

A capacitor with a capacitance of C Farads and a voltage drop of v Volts across its terminals stores an electric charge of q Coulombs on one plate and $-q$ Coulombs on the other plate.

$$q = C \cdot v$$

The voltage across the capacitor and the current through the capacitor are connected by means of a nonlinear, differential equation:

$$i = C\frac{dv}{dt}$$

The variation speed of the voltage determines the current through the capacitor, and this current is proportional with the value of the capacitance. For instance, if C = 1 F, the variation speed of the voltage is 1 V/s, and the current is 1 A. In other words, if a 1 A current goes through a 1 F capacitor, the voltage across the capacitor increases 1 V each second.

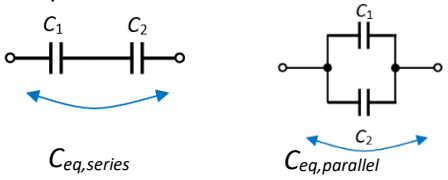
Steep variations of the voltage across the capacitor would require an infinite current through the capacitor. Any steep variation in the potential on one plate of the capacitor is entirely transmitted to the other plate.

1.3.2 Capacitor connections

By connecting two capacitors in series (Fig.1.24. a), or in parallel (Fig.1.24. b), the equivalent capacitance is:

$$C_{eq,series} = \frac{C_1 \cdot C_2}{C_1 + C_2}; \quad C_{eq,parallel} = C_1 + C_2$$

The equivalent capacitance of two capacitors connected in series (parallel) is always smaller (greater) than either of the two capacitors.



a) b)

Fig.1.24. Capacitor connections a) series; b) parallel.

1.3.3 The dc behaviour

- RC circuit with a voltage source

To illustrate the dc behaviour of the capacitor, let us consider a simple circuit, consisting of a capacitor, a resistor, and a dc voltage source, in a series connection, as shown in Fig.1.25.

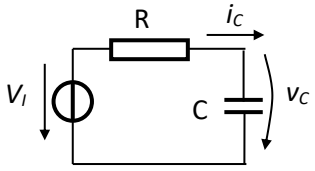


Fig.1.25. RC series circuit with a dc voltage source

The equations of the circuit are:

$$V_I = R \cdot i_C + v_C$$

$$i_C = C\frac{dv_C}{dt}$$

$$V_I = R \cdot C\frac{dv_C}{dt} + v_C$$

The non-homogenous first-order differential equation, to be solved for v_C, is:

$$R \cdot C\frac{dv_C}{dt} + v_C - V_I = 0$$

By using the boundary conditions:

$t = 0$; $v_C = v_C(0)$ - voltage across the capacitor at the initial time

$t = \infty$; $v_C = v_C(\infty)$ - voltage across the capacitor at the final time,

the solution is:

$$v_C(t) = v_C(0) \cdot e^{-\frac{t}{\tau}} + (1 - e^{-\frac{t}{\tau}}) \cdot v_C(\infty)$$

where $\tau = R \cdot C$ is the *time constant* of the circuit, measured in seconds (s).

For the circuit in Fig.1.25, the voltage across the capacitor is assumed to be $v_C(0) = 0$ V at the initial time (capacitor fully discharged). The final voltage, that is the voltage across the capacitor after an infinite time, is the voltage provided by the input voltage source, $v_C(\infty) = V_I$.

The equation that describes the time evolution of the voltage across the capacitor is:

$$v_C(t) = (1 - e^{-\frac{t}{\tau}}) \cdot V_I$$

The waveform of $v_C(t)$ is given in Fig.1.26. a).

After $t = \tau$, the capacitor is charged to 63% of the final value. The capacitor is said to be fully charged after a time $t = 5\tau$, when the voltage reaches 99% of the final value.

The time evolution of the current through the capacitor is shown in Fig.1.26. b).

$$i_C(t) = \frac{V_I - v_C(t)}{R}$$

The current thorough the capacitor is at the maximum value at the initial moment $i_C(0) = V_I/R$, since the entire voltage from the voltage source drops across R. Once the voltage across the capacitor increases, the current through the circuit decreases towards zero, after $t = 5\tau$. In a series RC circuit

supplied by a dc voltage source, once the transient regime $t \in (0; 5\tau)$ is completed, the capacitor enters the steady-state, or permanent regime, where the current through the capacitor is zero.

Note: The capacitor can be seen as an open circuit for dc signals once the transient regime is completed.

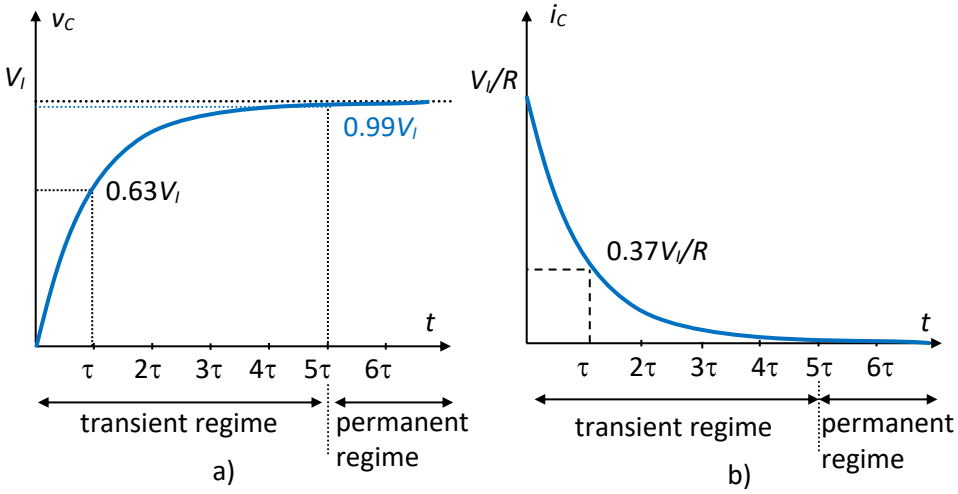


Fig.1.26. Waveforms for the circuit in Fig.1.25
a) voltage across the capacitor b) current through the capacitor.

- Charging the capacitor at a constant current

To analyse how the capacitor charges at a constant current, the circuit in Fig.1.27 is used, consisting of a capacitor and a dc current source.

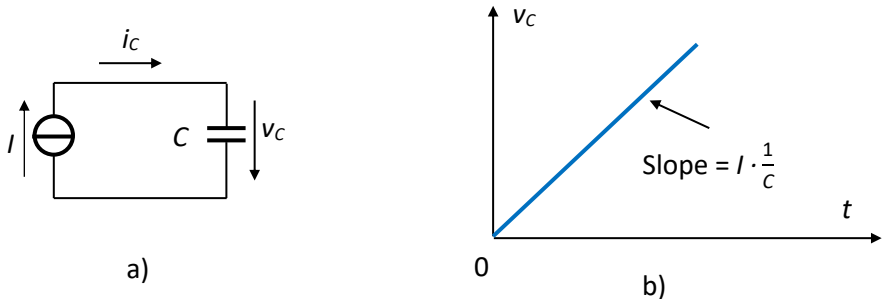


Fig.1.27. Charging the capacitor at constant current
a) schematic; b) voltage across the capacitor.

The voltage across the capacitor is assumed to be $v_C(0) = 0$ V at the initial moment (capacitor fully discharged). The current thorough the capacitor is constant $i_C(t) = I$, so the equations for the circuit are:

$$v_C(t) = \frac{1}{C}\int_0^t i_C(t)dt$$

$$v_C(t) = I \cdot \frac{1}{C} \cdot t$$

The voltage across the capacitor exhibits a linear increase over time (Fig.1.27. b). After a certain amount of time, since the voltage across the capacitor keeps increasing, either the capacitor or the current source may be damaged or even destroyed. If at some point, the direction of the current is reversed, the capacitor will discharge.

1.3.4 The ac behaviour

For certain frequencies of the input signal, the capacitor charges/discharges completely. This happens when the half-period of the signal is greater than the duration of the transient regime ($T/2 > 5\tau$). For the circuit in Fig.1.28, consisting of a series connection between a capacitor, a resistor and a voltage source, the time evolution of the voltage across the capacitor is depicted in Fig.1.29. a).

For the same circuit, if $T/2 < 5\tau$, the capacitor no longer manages to completely charge/discharge, as seen in Fig.1.29. b).

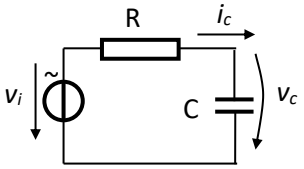


Fig.1.28. RC series circuit with ac voltage source

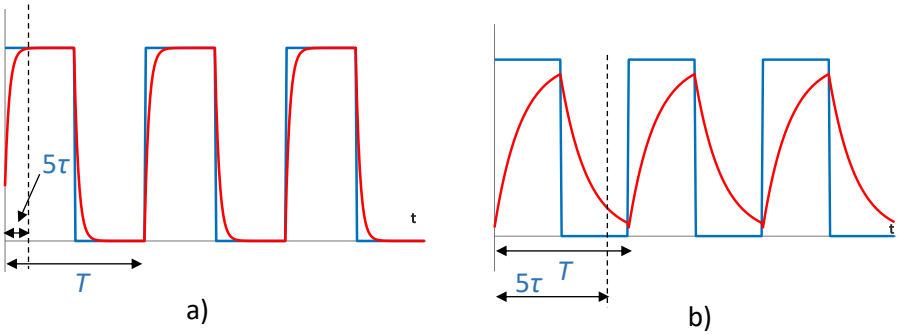


Fig.1.29. Voltage across a capacitor in ac
a) complete charging/discharging; b) partial charging/discharging.

Circuits that contain capacitors behave differently at different frequencies, since capacitors are *reactive* circuit elements. Its reactance is denoted X_C and shows the resistance of the capacitor in ac:

$$X_C = \frac{1}{2 \cdot \pi \cdot f \cdot C}$$

where f is the frequency of the signal. An increase in frequency determines a decrease in its reactance. Reactance is measured in ohms (Ω), just like any resistance.

Another term used when analysing the behaviour of reactive elements in ac is the *impedance*, denoted Z. Impedance is a general term, which describes the *"general resistance"*, while reactance is the imaginary part of the impedance. The impedance is expressed as a complex number, the sum between the real and the imaginary part.

$$Z = R + j \cdot X$$

For an ideal resistor, the impedance is equal to the resistance, $Z = R$.

For the capacitor, the capacitive impedance Z_C shows the value of the resistance in dc and ac:

$$Z_C = R - j \cdot X_C$$

The real part of the impedance is R (resistance in dc), and for the imaginary part $j = \sqrt{-1}$ represents the 90° phase shift between current and voltage, in a circuit with capacitors. For an ideal capacitor ($R = 0$), the impedance is a complex number that depends on the frequency of the signal:

$$Z_C = -j \cdot X_C = \frac{1}{j \cdot X_C} = \frac{1}{j \cdot 2 \cdot \pi \cdot f \cdot C}$$

The reactance X_C decreases when the frequency f increases. Thus, in dc, where $f = 0$ Hz, a capacitor is equivalent with an open circuit, $X_C \to \infty$.

1.4 Logarithmic scale

Since the range of values for the frequencies of an input signal in a circuit can span from Hz to MHz or even GHz, using a linear scale becomes almost impossible. This is the reason why a logarithmic scale is often employed for the graphical representations of circuit functions with respect to frequency, such as the transfer function. For the circuit in Fig.1.28, assuming R and C are ideal components, the complex transfer function is:

$$F(j\omega) = \frac{v_O(j\omega)}{v_I(j\omega)}$$

$$v_O(j\omega) = \frac{Z_C}{Z_R + Z_C} \cdot v_I(j\omega)$$

$$F(j\omega) = \frac{Z_C}{Z_R + Z_C} = \frac{\frac{1}{j\omega C}}{R + \frac{1}{j \cdot \omega \cdot C}} = \frac{1}{1 + j \cdot \omega \cdot R \cdot C}$$

The transfer function of a circuit is a complex number, defined by its *magnitude* and *phase*. Both magnitude and phase are expressed as functions of the *angular frequency*, $\omega = 2 \cdot \pi \cdot f$.

$$\text{Magnitude: } |F(j\omega)| = \frac{1}{\sqrt{1 + (\omega \cdot R \cdot C)^2}}$$

$$\text{Phase: } \Phi(\omega) = -\operatorname{arctg}(\omega \cdot R \cdot C)$$

The logarithmic scale provides the great advantage of expanding small values and compressing larger values (Fig.1.30). The origin of the axes is the unity. The values on the axis are written as powers of 10, and the interval between two consecutive values (called a *decade*) is the decimal logarithm of the two values. Six decades are depicted in Fig.1.30.

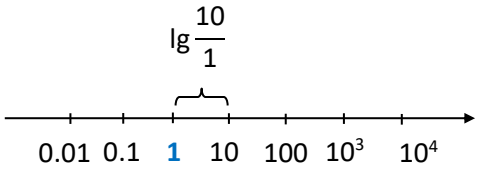


Fig.1.30. Logarithmic scale

When representing the magnitude of the transfer function, the horizontal axis is either the frequency or the angular frequency, in logarithmic scale.

- Decibel

For the vertical axis of the magnitude of the transfer function, values can be expressed either as ratios, $|F(jw)|$, or as *decibels*, the logarithm of the ratio, $|F(jw)|_{dB}$.

$$|F(jw)|_{dB} = 20 \cdot \lg|F(jw)|$$

If the output signal is equal to the input, then $|F(jw)| = 1$, the magnitude in dB is $|F(jw)|_{dB} = 0$. For an amplifier, $|F(jw)|_{dB}$ is positive, whereas for an attenuator, $|F(jw)|_{dB}$ is negative.

Chapter 2

DIODES

In this chapter, you will learn:

- the physical structure and the operation of the *pn* junction
- the current-voltage characteristic and the operating regions of semiconductor diodes
- the parameters of diodes and diode models
- how circuits with diodes are analysed
- applications of diode circuits
- Zener diodes, LEDs and photodiodes.

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2.1 The *pn* junction

The simplified physical structure of a *pn* junction is depicted in Fig.2.1.

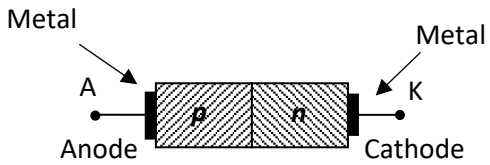


Fig.2.1. Simplified physical structure of the *pn* junction

The *pn* junction consists of two semiconductor regions, *p* and *n*, which are usually part of the same silicone crystal. In other words, a *pn* junction is created by positively (for the *p*-type region) and negatively (for the *n*-type region) doping regions of the same crystal. Metal contacts (usually aluminium) are used to connect the *p* and *n* regions to external wires. Silicon (Si), germanium (Ge), gallium arsenide (GaAs) are the semiconductor materials most used to build *pn* junctions.

In the *p*-type region, the crystal is doped with acceptor impurities, meaning that it contains an excess of holes (positive charge). In the *n*-type region, the crystal is doped with donor impurities,

meaning that it contains an excess of free electrons (negative charge). When the *pn* junction is not biased (open terminals, no applied voltage), the free carriers are unevenly distributed in the semiconductor crystal – there is an an excess of holes in the *p*-type region and an excess of free electrons in the *n*-type region, as shown in Fig.2.2.

Because the concentration of positive carriers is high in the *p* region and low in the *n* region, the holes diffuse (move) from the *p* side of the crystal to the *n* side. The holes that diffuse across the junction quickly recombine with some free electrons from the *n* region and are neutralized. The positive charge that remains un-neutralized is said to be *uncovered*. This recombination process takes place close to the junction and results in a region that lacks free electrons (is depleted of free electrons) and contains uncovered bound positive charge.

In a similar way, the electrons diffuse from the *n* side to the *p* side. The ones that recombine with the holes are neutralized, while some electrons remain *uncovered,* creating a region close to the junction that is depleted of holes and contains uncovered bound negative charge, as seen in Fig.2.2.

The depletion region is present on both sides of the junction. The positive and negative charges on both sides of the depletion region determine an electric field *E* across the region. This electric field opposes the diffusion of carriers from one side to the other, creating an equilibrium.

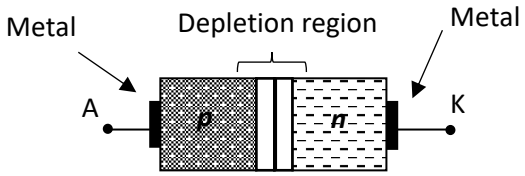


Fig.2.2. The *pn* junction with no applied voltage

The metal contacts outside the two regions are used to connect the *pn* junction in a circuit. If the *pn* junction is used as a diode, the terminals are called *Anode* (A) and *Cathode* (K), as shown in Fig.2.1 and Fig.2.2.

Based on the sign and value of the voltage applied at the terminals of the *pn* junction, the depletion region becomes narrower for forward biasing (Fig.2.3. a) or wider for reverse biasing (Fig.2.3. b). Forward biasing means that the voltage applied at the terminal connected to the *p* region (anode) is greater than the voltage applied to the terminal connected to the *n* region (cathode). Since the depletion region is narrow, more holes diffuse from the *p* region to the *n* region and more electrons diffuse from the *n* region to the *p* region.

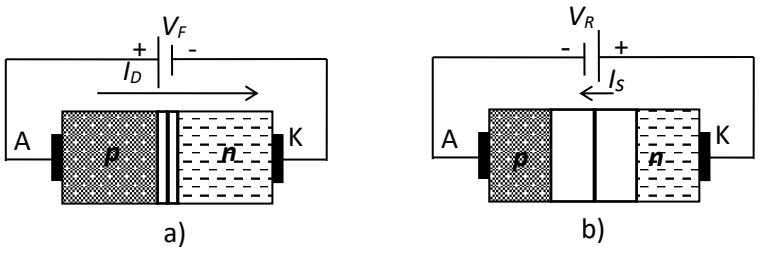


Fig.2.3. The *pn* junction in a) forward biasing; b) reverse biasing.

The movement of the carriers forms the diffusion current, I_D, whose direction is from the *p* side to the *n* side (Fig.2.3. a). Reverse biasing means that the voltage applied at the terminal connected to the *n* region (cathode) is greater than the voltage applied to the terminal connected to the *p* region (anode). Since the depletion region is wide, less holes diffuse from the *p* region to the *n* region and less electrons diffuse from the *n* region to the *p* region.

The movement of the carriers forms the drift current, I_S, whose direction is from the *n* side to the *p* side (Fig.2.3. b). The drift current I_S is significantly smaller than the diffusion current I_D, or, in other words, the *pn* junction conducts substantial current when forward biased, and almost no current when reverse biased.

When the *pn* junction is used as a diode (*D*), the circuit symbols are the ones in Fig.2.4. Notice that only the diffusion current I_D is shown, together with the positive voltage drop across the diode, V_D, from anode to cathode.

Fig.2.4. Semiconductor diode
a) symbol; b) symbol and positive directions for voltage and current.

2.2 Semiconductor diodes

2.2.1 The current-voltage characteristic of the silicon diode

Most diodes today are made of silicon, thus this chapter describes the properties of silicon diodes. The current-voltage characteristic $i_D(v_D)$ of the silicon diode is presented in Fig.2.5. A more detailed representation is given in Fig.2.6, where the horizontal axis is compressed for negative values and the vertical axis is expanded for negative values, to emphasize some key features.

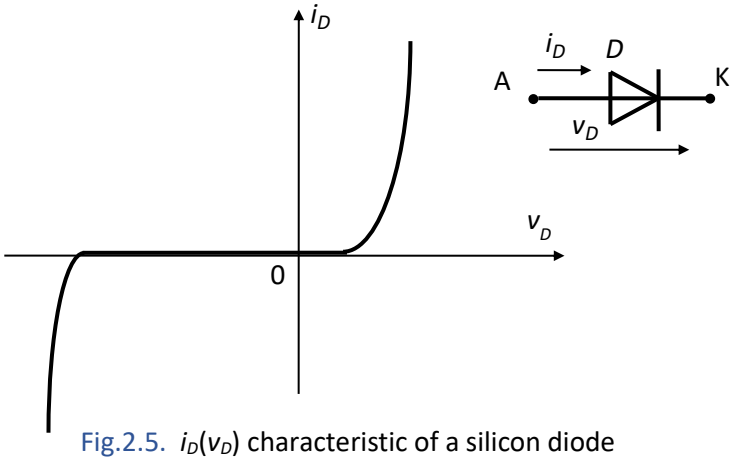


Fig.2.5. $i_D(v_D)$ characteristic of a silicon diode

On the horizontal axis, V_{Th} is the *threshold voltage* (*cutt-in voltage*) and it represents the minimum voltage needed by the diode in order to conduct a significant current. The typical value is V_{Th} = 0.5 V to 0.6 V, and for a fully conducting diode, the voltage drop is between 0.6 V and 0.8 V, with 0.7 V mostly used. For different types of diodes, at the same voltage drop of 0.7 V, the current through the diode can be 2 mA (small signal diodes) or 1 A (high power diode). The breakdown voltage, denoted V_{ZK} or V_{Br}, is the voltage for which the reverse current through the diode exhibits a rapid increase, that can be destructive for the diode. The breakdown voltage usually resides in the low negative values, e.g. V_{ZK} = -100 V for the 1N4148 diode.

Three operating regions are visible on the characteristic, based on the values of v_D, as follows: the forward bias region, where $v_D > 0$; the reverse bias region, where $v_D < 0$the breakdown bias region,

where $v_D < V_{ZK}$.

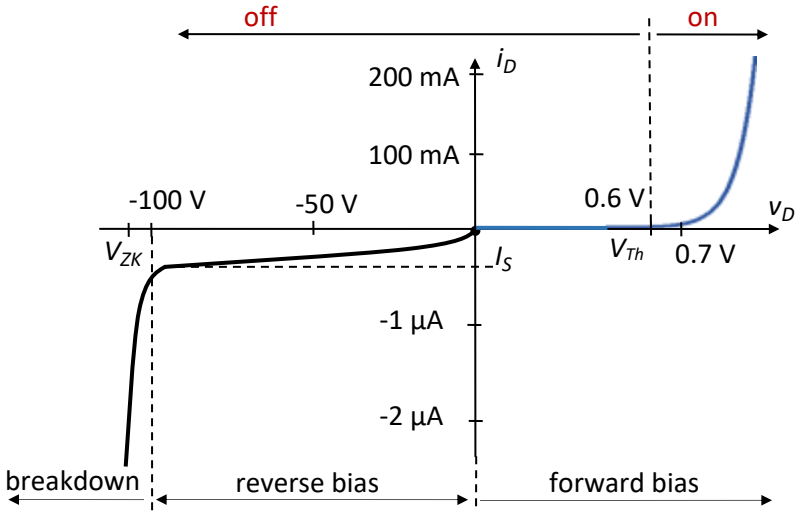


Fig.2.6. $i_D(v_D)$ characteristic of a silicon diode with expanded negative current scale and compressed negative voltage scale.

- The forward bias region

The diode is in the forward bias region or operates in forward bias when $v_D > 0$, i.e. the voltage in the anode is greater than the voltage in the cathode ($v_A > v_K$). To bring the diode into *on* state, v_D also needs to be above the threshold voltage V_{Th}. If v_D is positive, but lower than V_{Th}, the diode remains *off*, and the current I_D is insignificant (can be considered null).

For a silicon diode in forward bias, the equation that describes the relationship between i_D and v_D is William Shockley's exponential law, postulated in 1949:

$$i_D = I_S(e^{\frac{v_D}{n \cdot V_T}} - 1)$$

where:

I_S - *saturation current* or *scale current* – the current through the diode, from cathode to anode, in reverse bias, with values below -1 µA. The value of I_S is strongly influenced by temperature. As rule of thumb, I_S doubles in value for every 5°C increase in temperature.

n – *ideality factor* or *quality factor*, with a value between 1 and 2, depending on the fabrication process and the materials used. For a *pn* junction in a transistor, n is considered 1, whereas for a *pn* junction in a diode, n is between 1.6 for integrated diodes (fabricated using standard processes) and 2 for discrete diodes (which exhibit more non-idealities). Throughout this book, n = 2 will be used, unless otherwise specified.

V_T - thermal voltage, computed as:

$$V_T = \frac{K \cdot T}{q}$$

$K = 1.38 \cdot 10^{-23}$ J/K - Boltzman's constant

T = absolute temperature in kelvins (K) = 273 + temperature in °C

$q = 1.602 \cdot 10^{-19}$C – the magnitude of electronic charge.

At room temperature (20°C), V_T = 25.3 mV. When the ambient temperature is higher (25°C), the thermal voltage becomes V_T = 25.8 mV. For the sake of simplicity, V_T is approximated to 25 mV.

For significant values of I_D ($I_D >> I_D$), the exponential equation of the diode in forward bias is approximated to:

$$i_D \approx I_S \cdot e^{\frac{v_D}{n \cdot V_T}}$$

For two points on the $i_D(v_D)$ characteristic of a discrete diode (known as *quiescent points*), the equations are:

$$I_{D1} \approx I_S \cdot e^{\frac{V_{D1}}{n \cdot V_T}}$$
$$I_{D2} \approx I_S \cdot e^{\frac{V_{D2}}{n \cdot V_T}}$$
$$\frac{I_{D2}}{I_{D1}} \approx e^{\frac{V_{D2}-V_{D1}}{n \cdot V_T}}$$
$$V_{D2} - V_{D1} \approx n \cdot V_T \cdot \ln \frac{I_{D2}}{I_{D1}}$$
$$V_{D2} - V_{D1} \approx 2.3 \cdot n \cdot V_T \cdot \log \frac{I_{D2}}{I_{D1}}$$

The final equation shows that ten times increase of the current through the discrete diode determines a ($4.6 \cdot V_T$) increase in the voltage across the diode, that is approximately 120 mV at 25°C. For a transistor, the increase in voltage is halved, as $n = 1$.

The temperature dependence is best observed in the forward bias region of the $i_D(v_D)$ characteristic. The temperature influences two terms in Shockley's exponential law for i_D: the thermal voltage V_T and the saturation current I_S. The higher the temperature, the bigger the current through the diode, at a constant voltage across the diode v_D.

For a constant current thorough the diode, the voltage across the diode v_D decreases with temperature increase. In other words, there is a *negative temperature coefficient* (NTC), an increase of 1°C determines a decrease of v_D by 2 mV (Fig.2.7). The temperature is the temperature of the junction and is usually above ambient temperature.

For a constant i_D, v_D is computed as:

$$v_{D(T_2)} = v_{D(T_1)} + (-2\ \text{mV/°C}) \cdot (T_2 - T_1)\Big|_{I_D\text{-cst}}$$

where T_1, T_2 – temperature in °C.

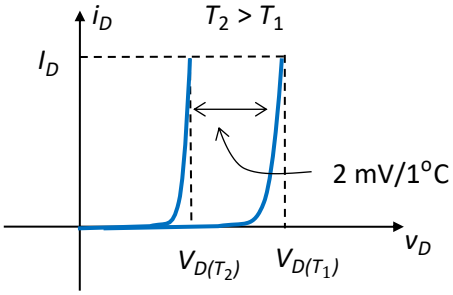


Fig.2.7. $i_D(v_D)$ characteristic of the *pn* junction for different temperatures

Examples	
1. Determine is the operating region (*forward bias*/*reverse bias*/*breakdown*) and the state (*on*/*off*) of the silicon diode for the following (V_D; I_D) pairs: i) (0.2 V; 1 nA) ii) (-10 V; -2.3 nA) iii) (-100 V; 2 µA).	

Solution:
i) the diode is in *forward bias* ($v_D > 0$ V), and the state is *off*.
ii) the diode is in *reverse bias* ($v_D < 0$ V), and the state is *off*.
iii) the diode is in *breakdown*.

2. Compute the current i_D through a discrete diode at room temperature, if v_D = 0.7 V and I_S = 2.5 nA. What is the operating region and the state of the diode?

Solution:
At room temperature, V_T = 25 mV. The current i_D is compute using Shockley's equation:

$$i_D = I_S \cdot (e^{\frac{v_D}{n \cdot V_T}} - 1)$$
$$i_D = 2.5 \cdot 10^{-9} \cdot (e^{\frac{0.7}{2 \cdot 25 \cdot 10^{-3}}} - 1)$$
$$i_D = 2.5 \cdot 10^{-9} \cdot (e^{14} - 1)$$
$$i_D = 2.5 \cdot 10^{-9} \cdot 1.15 \cdot 10^{6}$$
$$i_D = 2.87 \text{ mA}$$

The diode is in *forward bias* ($v_D > 0$ V) and since v_D is above the threshold voltage (0.6 V) and i_D is positive and significant (mA), the diode is *on*.

3. Compute the voltage v_D for a discrete diode at room temperature if i_D = 90 mA and I_S = 3 nA. What is the operating region and the state of the diode?

Solution:
Since i_D is given, v_D is computed using Shockley's equation:

$$i_D = I_S \cdot (e^{\frac{v_D}{n \cdot V_T}} - 1)$$
$$e^{\frac{v_D}{n \cdot V_T}} = \frac{i_D + I_S}{I_S}$$
$$\frac{v_D}{n \cdot V_T} = \ln\left(\frac{i_D}{I_S} + 1\right)$$
$$v_D \approx n \cdot V_T \cdot \ln\frac{i_D}{I_S}$$
$$v_D \approx 2 \cdot 25 \cdot 10^{-3} \cdot \ln\frac{90 \cdot 10^{-3}}{3 \cdot 10^{-9}}$$
$$v_D \approx 2 \cdot 25 \cdot 10^{-3} \cdot \ln 30 \cdot 10^{6}$$
$$v_D \approx 50 \cdot 10^{-3} \cdot 17.21$$
$$v_D \approx 0.86 \text{ V}$$

The diode is in *forward bias* ($v_D > 0$ V) and since v_D is above the threshold voltage (0.6 V) and i_D is positive and significant (tens of mA), the diode is *on*.

4. Compute v_D on the *pn* junction at a temperature of 40°C, if v_D = 0.7 V at 20°C.

Solution:

$$v_{D(T_2)} = v_{D(T_1)} + (-2 \text{ mV/°C}) \cdot (T_2 - T_1)\Big|_{I_D\text{-cst}}$$
$$v_{D(T_2)} = 700 \text{ mV} + (-2 \text{ mV/°C}) \cdot 20°\text{C}$$
$$v_{D(T_2)} = 700 \text{ mV} - 40 \text{ mV} = 660 \text{ mV} = 0.66 \text{ V}$$

- The reverse bias region

The diode is in the reverse bias region or operates in *reverse bias* for $v_D < 0$ V ($v_A < v_K$). From the diode's exponential equation, for a negative v_D, with an absolute value several times greater than V_T, the exponential term can be neglected with respect to 1, and the current through the diode becomes:

$$i_D \approx - I_S$$

In reverse bias, i_D is significantly lower (nA, pA) than the current through the diode in forward bias (tens, hundreds of mA), thus the current in reverse bias can be considered null. In real circuits, the absolute value of the current through the diode in reverse bias is above I_S, but still too small to be taken into account, e.g. if I_S is a few pA, then I_D is a few nA.

- The breakdown region

The *breakdown* occurs when the reverse voltage drop across the diode ($v_{DR} = - v_D$) is above a certain voltage, specific to each type of diode. The breakdown voltage is denoted V_{ZK} or V_{Br}, as shown in Fig.2.5 and Fig.2.6 (third quadrant). If the reverse voltage drop across the diode is above the absolute value of the breakdown voltage ($v_{DR} > |V_{ZK}|$ or $v_D < V_{ZK}$), the diode is in the breakdown region.

In the breakdown region, the current through the diode is rapidly increasing (steep slope of the characteristic). The power dissipated by the diode is also high, and the diode may be destroyed. To avoid this phenomenon, the current through the diode must be limited by the exterior circuit at a low, safe value. In practice, diodes are not used in circuits where the breakdown voltage can be exceeded.

However, there is a special type of diodes that are designed to be used in the breakdown region – the Zener diodes, to be studied in a subsequent section.

Problems

1. Determine is the operating region (*forward bias*/*reverse bias*/*breakdown*) and the state (*on*/*off*) of the silicon diode for the following (V_D; I_D) pairs:
i) (0.75 V; 30 mA)
ii) (0.75 V; -1.3 nA)
iii)(-105 V; -1 µA)
iv) (0.2 V; 2 µA).

2. Compute the current i_D through a discrete diode at room temperature, for $v_D = 0.8$ V and $I_S = 3$ nA. What is the operating region of the diode?

3. Compute the current i_D through an integrated diode at a temperature $T = 25^oC$, if $v_D = 0.8$ V and $I_S = 3$ nA. What is the operating region of the diode?

4. Compute the voltage v_D across a discrete diode at room temperature, for $i_D = 100$ mA and $I_S = 4$ nA. What is the operating region of the diode?

5. Compute the voltage v_D across an integrated diode at room temperature, for $i_D = 80$ mA and $I_S = 6$ nA. What is the operating region of the diode?

6. Compute the voltage drop across a *pn* junction at a temperature of 35^oC, if the voltage drop at 10^oC is 0.67 V.

2.2.2 Connecting diodes in a circuit

To determine the current through a diode, i_D, and the voltage across the diode, v_D, the diode must be connected in a circuit. If a circuit consists only of a voltage source and a diode, the current through

the diode is theoretically infinite, which destroys the diode. Thus, a resistor is always to be included in such a circuit. The simple series circuit with a diode and a resistor (a *DR* circuit) is shown in Fig.2.8.

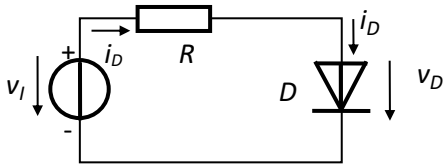


Fig.2.8. Simple *DR* circuit

Computing i_D and v_D begins with writing down the circuit's equations: Shockley's equation, Kirchhoff's voltage and current laws, and Ohm's law. Since the circuit's elements are connected in series, there is a single current through the circuit, i_D.

$$\text{Shockley's equation: } i_D = I_S \cdot e^{\frac{v_D}{n \cdot V_T}}$$

$$\text{Load line equation: } v_I = i_D \cdot R + v_D$$

Assuming I_S, n and V_T are given, the system contains two unknowns, namely i_D and v_D. The exponential equation makes it impossible to solve the system using substitution, so other methods are employed: the graphical method, or the analytical method.

- Graphical method

The graphical method consists of a graphical representation of the circuit's equations; the solution (V_D; I_D) is the intersection between the two graphs, as depicted in Fig.2.9. This point is known as the *quiescent point* or *bias point* or *dc operating point*, denoted *Q*. Any changes in the circuit (different value of the input voltage, different diode, different resistor), the quiescent point also changes. The pair of values in the quiescent point are instantaneous values of i_D and v_D, denoted $Q(V_D, I_D)$.

The graphical representation of the linear circuit equation is a line, also known as the *load line* (denoted *d* in Fig.2.9). For Shockley's equation, the graph is exponential.

The intersection between the load line with the two axes is given by the value of V_I, on the horizontal axis (for $i_D = 0$ mA), and V_I/R on the vertical axis (for $v_D = 0$ V).

For a different value of *R*, e.g. $R_1 < R$, the intersection between the new load line d_1 and the horizontal axis remains unchanged, but the intersection with the vertical axis is now higher than for the load line, *d*. The new quiescent point Q_1 is located higher on the exponential curve than the previous *Q*, with both values changed ($I_{D1} > I_D$ and $V_{D1} > V_D$).

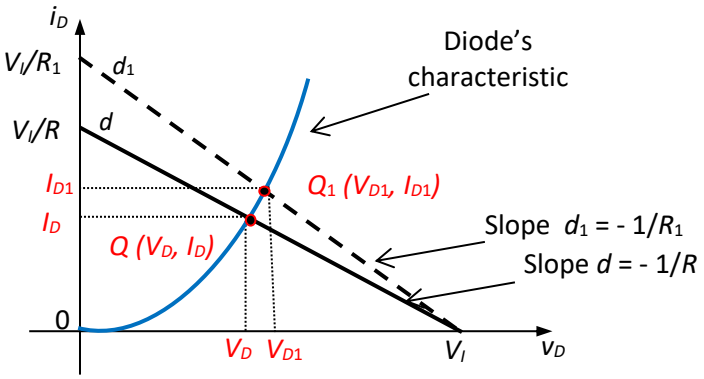


Fig.2.9. Graphical method for solving a simple *DR* circuit

- Analytical method (substitution method)

Determining i_D and v_D using the analytical method begins by considering an initial value for v_D, for which the diode is in on state. Successive substitutions will lead to the values of i_D and v_D. The steps to be applied when using the analytical method are:

- Step 1 – initial value for v_D when the diode is in on state $V_D = 0.7$ V
- Step 2 – using V_D from Step 1, compute I_D from the load line equation
- Step 3 – recompute V_D from Shockley's equation.

These steps represent the first iteration of the analytical method. The first iteration provides a good enough approximation of i_D and v_D. If more precision is required, the second and third steps can be repeated multiple times; one can stop when the values for i_D and v_D no longer change significantly between successive iterations.

Example

Compute i_D and v_D using the analytical method for the circuit in Fig.2.8, for $V_I = 4$ V, $R = 1.5$ kΩ, and the diode D is 1N4148, with $I_S = 4$ nA and $n = 2$.

Solution:

First iteration

Step 1 – assume $V_D = 0.7$ V

Step 2 – find I_D from the load line equation:

$$I_D = \frac{V_I - V_D}{R}$$

$$I_D = (4 - 0.7)/1.5 \text{ mA}$$

$$I_D = 2.2 \text{ mA}$$

Step 3 – replace I_D in the diode's equation:

$$I_D = I_S \cdot (e^{\frac{V_D}{n \cdot V_T}} + 1)$$

$$V_D \approx n \cdot V_T \cdot ln \frac{I_D}{I_S}$$

$$V_D \approx 2 \cdot 25 \cdot 10^{-3} \cdot \ln \frac{2.2 \cdot 10^{-3}}{4 \cdot 10^{-9}}$$

$$V_D \approx 50 \cdot 10^{-3} \cdot \ln (0.55 \cdot 10^{6})$$

$$V_D \approx 50 \cdot 10^{-3} \cdot 13.21$$

$$V_D \approx 0.66 \text{ V}$$

For more precise values, the solution continues with the second iteration.

Second iteration

$$I_D = (4 - 0.66)/1.5 \text{ mA}$$

$$I_D \approx 2.23 \text{ mA}$$

$$V_D \approx 2 \cdot 25 \cdot 10^{-3} \cdot \ln \frac{2.23 \cdot 10^{-3}}{4 \cdot 10^{-9}}$$

$$V_D \approx 50 \cdot 10^{-3} \cdot \ln (0.557 \cdot 10^{6})$$

$$V_D \approx 50 \cdot 10^{-3} \cdot 13.23$$

$$V_D \approx 0.661 \text{ V}$$

The values for V_D and I_D exhibit insignificant changes between the two iterations, so the method stops here.

Problems

1. Determine i_D and v_D using the analytical method for the circuit in Fig.2.8, for V_I = 5 V, R = 3 kΩ, and the diode D is 1N4148, with I_S = 4 nA and n = 2. What is the operating region of the diode? Justify your answer.

2. Determine i_D and v_D using the analytical method for the circuit in Fig.2.8, for V_I = 7 V, R = 5 kΩ, and the diode D is 1N4148, with I_S = 4nA and n = 1.6. What is the operating region of the diode? Justify your answer.

3. Determine i_D and v_D using the analytical method for the circuit in Fig.2.8, for V_I = 8 V, R = 4.5 kΩ, and the diode D is 1N4148, with I_S = 4nA and n = 1.8. What is the operating region of the diode? Justify your answer.

2.2.3 Parameters of the diode

Modelling the behaviour of the diode is useful when analysing of diode circuits. The model of the diode can be simple, if only some of the diode's characteristics are considered, or a complex one, which includes more properties.

The behaviour of the diode is described by means of its parameters: static parameters and differential/dynamic parameters.

- Static parameters

Static parameters are computed in circuits where the input is a dc signal (voltage or current). Since there is a single value of the input signal, the diode operates in a single quiescent point, $Q(V_D, I_D)$. When the diode is on, both I_D and V_D are positive and non-zero. The static resistance r_D is computed as:

$$r_D = \frac{V_D}{I_D}$$

The diode can be modelled using its static resistance r_D. For a new quiescent point (different value of the input voltage, different diode, different resistor), the static resistance needs to be recomputed.

Since i_D and v_D are connected by means of an exponential law, a small variation of the voltage across the diode determines a significant variation of the current through the diode. This is the reason why, for the quiescent point $Q_1(V_{D1}, I_{D1})$ in Fig.2.9, the static resistance r_{D1} is lower than the static resistance r_D for quiescent point $Q(V_D, I_D)$.

The static conductance g_D can also be computed:

$$g_D = r_D^{-1} = \frac{I_D}{V_D}$$

Example

Compute the static resistance and conductance for a diode operating in the quiescent points:
a) Q_1(0.68 V; 20 mA)
b) Q_2 (0.55 V; 1.5 mA)
c) Q_3 (0.72 V; 80mA).

Solution:

$$r_D = \frac{V_D}{I_D}, \qquad g_D = \frac{I_D}{V_D}$$

a) $r_D = 0.68/20 \cdot 10^{-3}$ [Ω], $g_D = 1/r_D$ [S]

r_D = 34 Ω, g_D = 29.4 mS
b) r_D = 0.55 / 1.5 · 10^{-3} [Ω], r_D = 367 Ω, g_D = 2.7 mS
c) r_D = 0.72 / 80 · 10^{-3} [Ω], r_D = 9 Ω, g_D = 111 mS

Problems

1. Compute the static resistance and conductance for a diode operating in the quiescent points:
a) Q_1(0.67 V; 15 mA)
b) Q_2(0.76 V; 25 mA)
c) Q_3(0.79 V; 100 mA)
d) Q_4(0.68 V; 44 mA).

- Dynamic parameters

In real circuits, any dc signal exhibits small variations, thus the diode operates not in a single quiescent point, but rather in a region on the diode's characteristic, centred around the particular quiescent point. The smaller the signal variations, the smaller the region around the quiescent point. In theory, the region on the diode's characteristic is considered linear, and the diode can be modelled using its dynamic or differential resistance. The circuit in Fig.2.10 is supplied with an ac input voltage (low amplitude) in series with a dc voltage source.

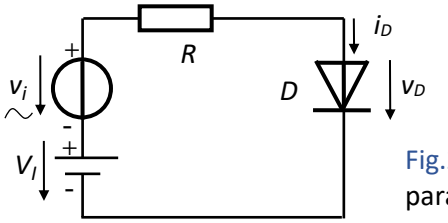


Fig.2.10. Circuit for computing the dynamic parameters of the diode

For a sinusoidal input voltage v_i, the variable signal is superimposed on the dc signal around the quiescent point Q, as seen in Fig.2.11.

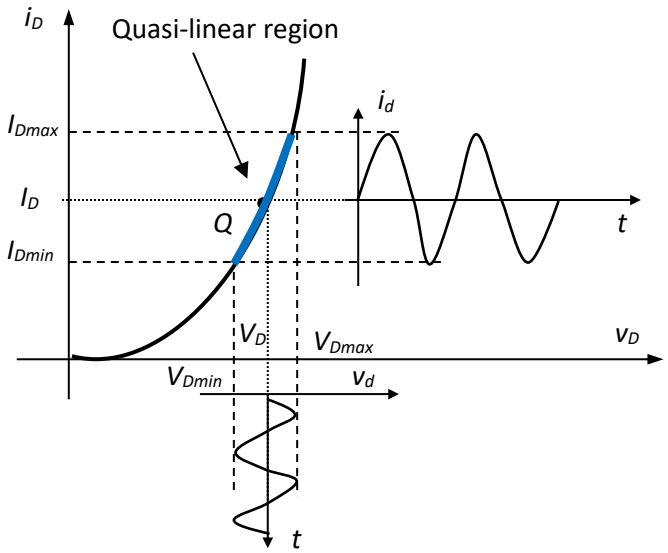


Fig.2.11. Superposition of variable signals on dc signals in the quasi-linear region around the quiescent point on the characteristic of a diode

The total instantaneous voltage across the diode, $v_D(t)$, consists of the dc component, V_D, and the ac component, $v_d(t)$ [1]:

$$v_D(t) = V_D + v_d(t)$$

$$i_D(t) = I_S \cdot e^{\frac{V_D + v_d(t)}{n \cdot V_T}} = I_S \cdot e^{\frac{V_D}{n \cdot V_T}} \cdot e^{\frac{v_d(t)}{n \cdot V_T}}$$

Using Shockley's equation, the dc current through the diode is:

$$I_D = I_S \cdot e^{\frac{V_D}{n \cdot V_T}}$$

whereas the ac current becomes:

$$i_D(t) = I_D \cdot e^{\frac{v_d(t)}{n \cdot V_T}}$$

If the amplitude of $v_d(t)$ is negligible and the power of e is much smaller than unity, the exponential equation can be solved using a Taylor series decomposition and considering the first two terms.

$$\widehat{V_d} \ll n \cdot V_T$$

Usually, the amplitude of $v_d(t)$ is a maximum of 10 mV for discrete diodes, with n = 2 and V_T = 25 mV, and a maximum of 5 mV [1] for transistors (where the *pn* junction is considered almost ideal and n = 1). The total instantaneous current through the diode and the variable component of the current are:

$$i_D(t) \approx I_D + I_D \cdot \frac{v_d(t)}{n \cdot V_T}$$

$$i_d(t) = \frac{I_D}{n \cdot V_T} \cdot v_d(t)$$

The ratio of $v_d(t)$ and $i_d(t)$ gives the *dynamic* or *differential* or *small-signal resistance*, r_d, computed as:

$$r_d = \frac{v_d(t)}{i_d(t)} = \frac{v_d(t)}{\frac{I_D}{n \cdot V_T} \cdot v_d(t)} = \frac{1}{\frac{I_D}{n \cdot V_T}} = \frac{n \cdot V_T}{I_D}$$

$$r_d = \frac{n \cdot V_T}{I_D}$$

The dynamic resistance also depends on the value of the current through the diode, I_D, in the quiescent point. The higher the current through the diode in the quiescent point, the lower the values of the static and dynamic resistances.

Another way to compute the dynamic resistance of the diode is by computing the inverse slope of the quasi-linear segment around the quiescent point. Two pairs of values are required for this, namely (V_{Dmax}, I_{Dmax}) and (V_{Dmin}, I_{Dmin}), as seen in Fig.2.11.

$$r_d = \frac{V_{Dmax} - V_{Dmin}}{I_{Dmax} - I_{Dmin}}$$

The dynamic conductance is computed as the inverse dynamic resistance:

$$g_d = \frac{I_D}{n \cdot V_T}$$

For the circuit in Fig.2.10, the diode can be modelled by its static resistance r_D, computed on the equivalent dc circuit, and its dynamic resistance r_d, computed on the ac equivalent circuit (small-signal circuit).

Example

Plot $v_I(t)$, $v_D(t)$ and $i_D(t)$ for the circuit in Fig.2.12, considering R_1 = 0.4 kΩ, R_2 = 10 Ω, V_I = 2 V, $v_i(t) = 10\sin\omega t$ [mV], I_S = 10 nA, V_T = 25 mV and n = 2.

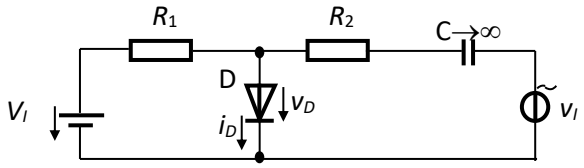


Fig.2.12. Circuit for computing the parameters of the diode

Solution:

The initial circuit is analysed in dc and in ac, using its equivalent versions.

The dc components of $v_D(t)$ and $i_D(t)$ are determined from the dc equivalent circuit, whereas the small-signal, variable components are computed using the the ac equivalent circuit.

$$v_D(t) = V_D + v_d(t)$$
$$i_D(t) = I_D + i_d(t)$$

The dc equivalent circuit is obtained by replacing the capacitor C with and open circuit and the diode D with its static resistance (Fig.2.13).

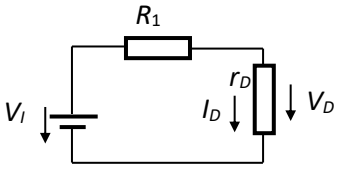


Fig.2.13. The dc equivalent circuit

The values of I_D and V_D in the quiescent point are computed using either the graphical or the analytical methods. For this circuit, the quiescent point is Q(0.63 V; 3.4 mA). The dc value of the voltage across the diode is V_D = 0.63 V, and the dc current though the diode is I_D = 3.4 mA.

The static resistance is:

$$r_D = \frac{0.63}{3.4 \cdot 10^{-3}} = 185.3\ \Omega$$

The ac equivalent circuit is obtained by replacing the capacitor C with a short-circuit, setting the dc voltage source to zero and replacing the diode with its dynamic resistance (Fig.2.14).

The dynamic resistance is:

$$r_d = \frac{2 \cdot 25 \cdot 10^{-3}}{3.4 \cdot 10^{-3}} = 14.7\ \Omega$$

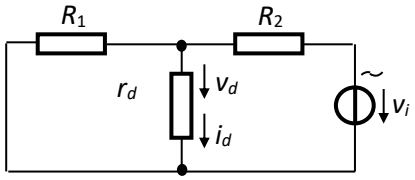


Fig.2.14. The ac equivalent circuit (small-signal)

The ac component of the voltage across the diode is computed using the voltage divider method, and the ac component of the current through the diode is determined using Ohm's law, as follows:

$$v_d(t) = \frac{r_d \,||\, R_1}{r_d \,||\, R_1 + R_2} \cdot v_i(t)$$

$$v_d(t) = \frac{14.7 \,||\, 400}{14.7 \,||\, 400 + 10} \cdot 10\sin\omega t$$

$$v_d(t) = \frac{14.1}{24.1} \cdot 10\sin\omega t$$

$$i_d(t) = \frac{v_d(t)}{r_d}$$

$$i_d(t) = \frac{v_d(t)}{14.7}$$

The final values of the ac components are:

$$v_d(t) \approx 5.8\sin\omega t \text{ [mV]}$$
$$i_d(t) \approx 0.4\sin\omega t \text{ [mA]}$$

and the complete expressions of the signals are:

$$v_D(t) = 630 + 5.8\sin\omega t \text{ [mV]} = 0.63 + 0.0058\sin\omega t \text{ [V]}$$
$$i_D(t) = 3.4 + 0.4\sin\omega t \text{ [mA]}.$$

The voltage drop across the diode varies between V_{Dmax} = 635.8 mV and V_{Dmin} = 624.2 mV, and the current through the diode varies between I_{Dmax} = 3.8 mA and I_{Dmin} = 3 mA. The waveforms of $v_I(t)$, $v_D(t)$ and $i_D(t)$ are shown in Fig.2.15.

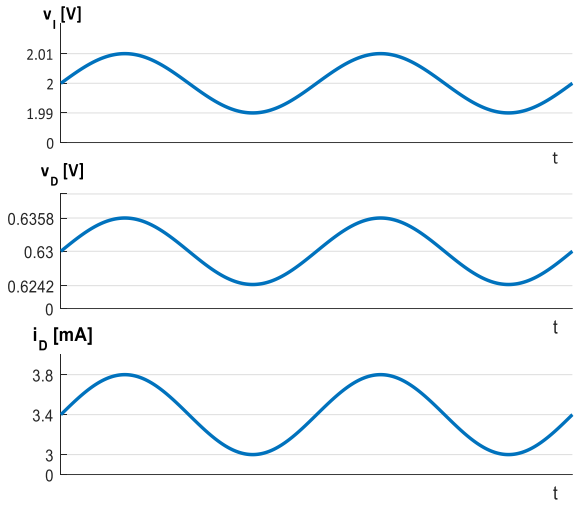


Fig.2.15. Waveforms of $v_I(t)$, $v_D(t)$ and $i_D(t)$

Problems

1. Plot $v_I(t)$, $v_D(t)$ and $i_D(t)$ for the circuit in Fig.2.12 for R_1 = 0.8 kΩ, R_2 = 16 Ω, V_I = 4 V, $v_i(t)$ = 8sinωt [mV], I_S = 10 nA, V_T = 25 mV and n = 2.

2. Plot $v_I(t)$, $v_D(t)$ and $i_D(t)$ for the circuit in Fig.2.12 for R_1 = 0.85 kΩ, R_2 = 20 Ω, V_I = 5 V, $v_i(t)$ = 5sinωt [mV], I_S = 4 nA, V_T = 20 mV and n = 2.

2.3 Diodes in switching regime

The exponential model of the diode, based in Shockley's equation, is used when the diode is in the *permanent conduction regime*, and it can be replaced by its equivalent static and dynamic resistances.

For a quick analysis of diode circuits, another model for the diode is employed, the *constant voltage drop model*. For this simple model of the diode, the *on* and *off* states are described by a constant value and a variable value (either constant i_D and variable v_D, or variable i_D and constant v_D).

2.3.1 The constant voltage drop model

The constant voltage drop model sets the voltage $v_D = 0.7$ V as the boundary between *on* and *off* states, and this will be the voltage drop across the diode in *on* state. The $i_D(v_D)$ characteristic of this model is now linear (Fig.2.16), as opposed to the exponential one in (Fig.2.5), and consist of two segments, one for *on* and another for the *off* state of the diode. The breakdown region is not shown in Fig.2.16.

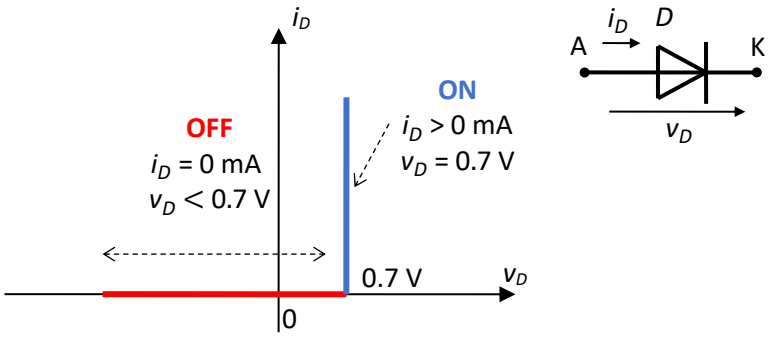


Fig.2.16. The $i_D(v_D)$ characteristic for the constant voltage drop model of the diode, $v_D = 0.7$ V

The equations for i_D and v_D in *on* and *off* states are valid for the standard (positive) directions of the current through the diode and the voltage drop across the diode (from anode to cathode).

When the diode is *on*, the voltage drop is constant, $v_D = 0.7$ V, while the current i_D is positive and determined by the other elements of the circuit.

When the diode is *off*, it acts as an open circuit (open switch), meaning the current i_D is null. The voltage across the diode v_D is determined by the other elements of the circuits, and stays below 0.7 V.

Special attention must be paid to the extreme values of the current through the diode ($I_{Dmax} < I_{Dmax}$) and the maximum reverse voltage across the diode ($V_{DR} < |V_{Br}|$), so that the diode is not destroyed.

The diode can be seen as a switch for current, since it either allows a current flow, in *on* state, or blocks the current flow, in *off* state. The equivalent circuit for the diode in *on* state is a closed switch in series with a 0.7 V dc source, whereas for the diode in *off* state, the switch is open (Fig.2.17).

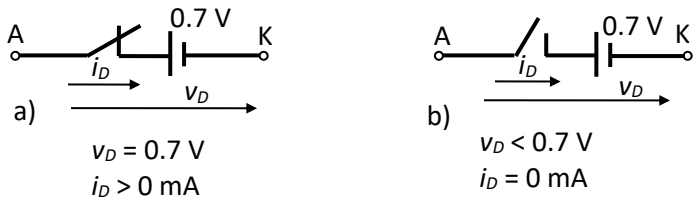


Fig.2.17. Constant voltage drop model of the diode, $v_D = 0.7$ V
a) *on* state; b) *off* state.

When electronic devices switch between two states, *on* and *off*, the devices are said to operate in the *switching regime*. The diode operates in the switching regime when the constant voltage drop model is used.

Example	
Specify the *on/off* state of the diode, assuming the constant voltage drop model: a) i_D = 0 mA and v_D = - 0.7 V b) i_D = 0 mA and v_D = - 5 V c) i_D = 30 mA and v_D = 0.7 V c) i_D = 72 mA and v_D = 0.7 V. **Solution:** a) the diode is *off*, because i_D = 0 mA and v_D < 0.7 V b) the diode is *off*, because i_D = 0 mA and v_D < 0.7 V c) the diode is *on*, because i_D > 0 mA and v_D = 0.7 V d) the diode is *on*, because i_D > 0 mA and v_D = 0.7 V.	

2.3.2 Analysis of *DR* switching two-port circuits

The circuits consisting of diodes and resistors, for which the diodes switch between *on* and *off*, are called *DR switching circuits*. The input and output of a circuit is called *port*, so circuits with one input and one output are hence called *two-port circuits* or *two-port networks*.

Four different two-port series circuits can be built using just one diode and one resistor, as shown in Fig.2.18. The positive directions for the voltage across the diode and the current through the diode are also specified on the schematics.

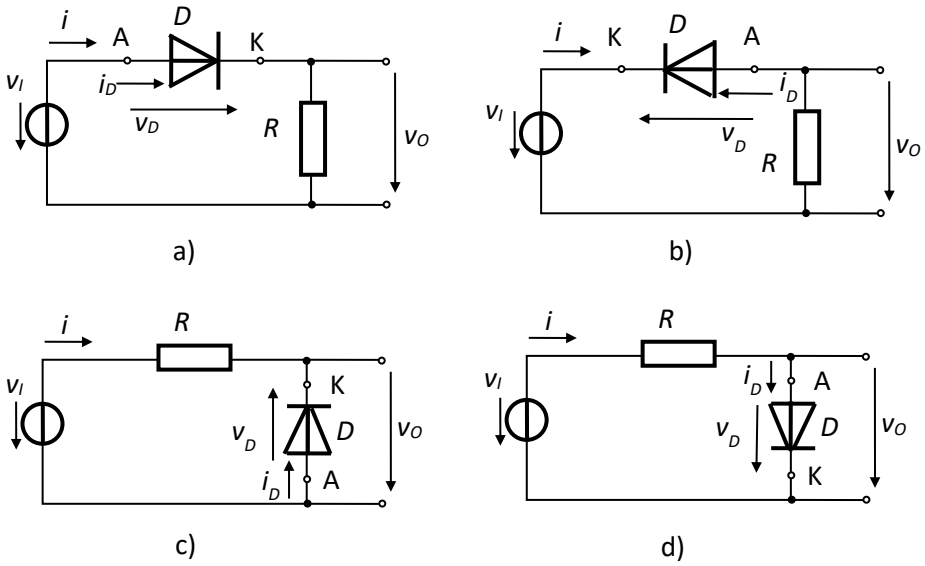


Fig.2.18. Two-port *DR* series circuits
a) and b) output measured across *R*; c) and d) output measured across *D.*

The analysis of *DR* switching two-port circuits, for which both input and output signals are voltages, means analysing the voltage transfer, $v_O(v_I)$, from input to output. The *voltage transfer characteristic* (VTC) is the graphical representation of $v_O(v_I)$.

For *DR* switching two-ports, the VTC $v_O(v_I)$ is a non-linear plot, with two segments, on for each state of the diode. To obtain the VTC $v_O(v_I)$, the expression of v_O and the range of values for v_I need to be determined, for each state of the diode, using the following steps:

Step 1 – write the circuit's equations, using Ohm's law, Kirchhoff's voltage law and Kirchhoff's current law.

Step 2 – draw the equivalent schematics for the *on* and *off* states of the diode, using the constant voltage drop model (Fig.2.17). For a *DR* circuit with one diode, there will be two equivalent schematics.

Step 3 – customize the circuit's equations written in Step 1 for each state of the diode, by using the values of v_D and i_D from the constant voltage drop model.

Step 4 – find v_O and the range of values for v_I, for the *on* and *off* states of the diode. Write the complete expression of $v_O(v_I)$.

Step 5 – plot the VTC $v_O(v_I)$.

Step 6 – based on the previously determined VTC $v_O(v_I)$, waveforms of $v_O(t)$ can be plotted, for any given $v_I(t)$.

For the circuit in Fig.2.18. a), the circuit equations are:

$$v_I = v_D + v_O$$
$$v_O = i_D \cdot R$$

When the diode is *on* (Fig.2.19. a), the output voltage is computed from the equivalent circuit:

$$v_O = v_I - 0.7$$
$$v_O > 0;\ v_I - 0.7 > 0;\ v_I > 0.7\ \text{V}$$

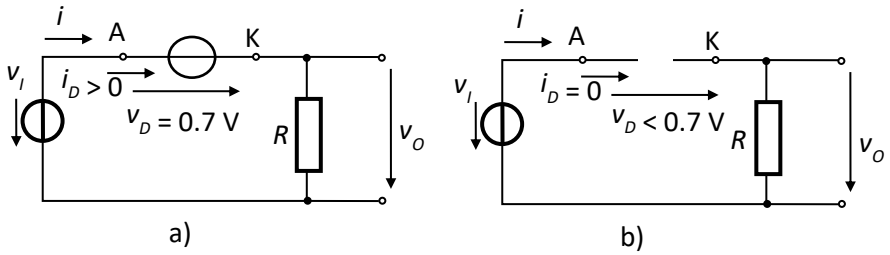


Fig.2.19. Equivalent schematic for the circuit in Fig.2.18. a)
a) *D - on*; b) *D – off.*

When the diode is *off* (Fig.2.19. b), the output voltage becomes:

$$v_O = 0\ \text{V}$$
$$v_I = v_D < 0.7\ \text{V}$$

The final expression of $v_O(v_I)$ is:

$$v_O = \begin{cases} 0, & v_I < 0.7\ \text{V} \\ v_I - 0.7, & v_I < 0.7\ \text{V} \end{cases}$$

The VTC $v_O(v_I)$ is plotted in Fig.2.20. a), where the two segments correspond to the two states of the diode. Sample waveforms for $v_I(t)$ and $v_O(t)$ are given in Fig.2.20. b). For circuits where the amplitude of $v_I(t)$ is much bigger than 0.7 V (tens, hundreds of volts), the voltage drop across the diode in *on* state can be neglected.

The circuits in Fig.2.18. a) and b) can be seen as half-wave voltage rectifiers since the output voltage is either null or (almost) equal to on half-wave of the input voltage: positive half-wave for the circuit in Fig.2.18. a), negative half-wave for the circuit in Fig.2.18. b).

The electrical function of the circuits in Fig.2.18 is voltage limiter or voltage clamp circuit, either superior or inferior, based on the orientation of the diode and whether the output is measured on the diode or on the resistor.

The circuit in Fig.2.18. c) limits the output voltage to – 0.7 V (inferior limiter or inferior clamp

circuit), whereas the circuit in Fig.2.18. d) limits the output voltage to 0.7 V (superior limiter or superior clamp circuit). By connected two or more diodes in series at the output of the circuit, the limit can be changed to multiples of 0.7 V or -0.7 V.

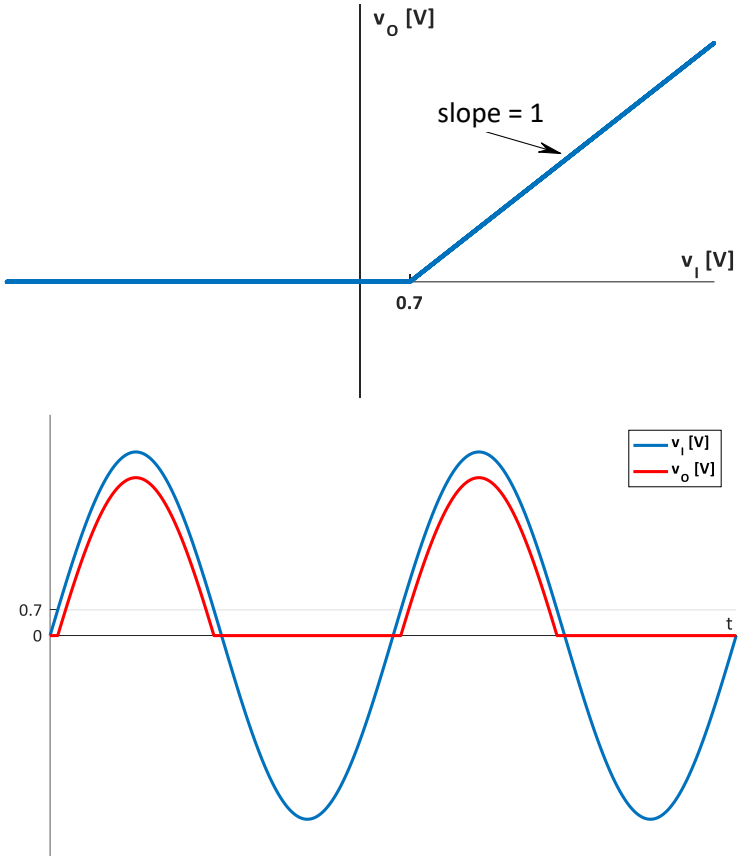


Fig.2.20. For the circuit in Fig.2.18. a)
a) VTC $v_O(v_I)$; b) sample waveforms for $v_I(t)$ and $v_O(t)$.

Example

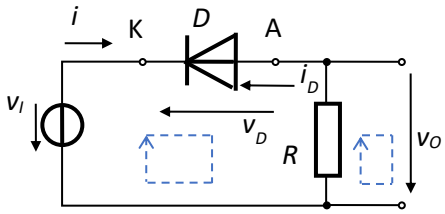
For the circuit Fig.2.18. b), using the constant voltage drop model:
a) deduce and plot the VTC $v_O(v_I)$ for $v_I \in$ [-10 V; 10 V],
b) specify the application of the circuit,
c) plot $v_I(t)$ and $v_O(t)$ for
i) $v_I(t) = 0.3\sin\omega t$ [V]
ii) $v_I(t) = 4\sin\omega t$ [V].
d) find the range of values for R, so that the current through the diode does not exceed I_{Dmax} = 30 mA and $v_I(t) = 4\sin\omega t$ [V].

Solution:

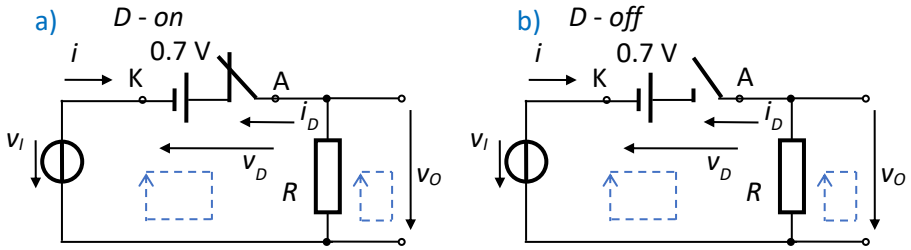
a) The circuit in Fig.2.18. b) is shown once again, this time with the chosen directions, clockwise (blue dotted line).
Step 1.
The circuit's equations are:

$$-v_I - v_D - i_D \cdot R = 0$$

$$v_O + i_D \cdot R = 0;\ v_O = -\ i_D \cdot R$$
$$-\ v_I - v_D + v_O = 0$$
$$i = -\ i_D$$



Step 2.
The equivalent schematic for the two states of the diode are:



$v_D = 0.7$ V
$i_D > 0$ mA

$v_D < 0.7$ V
$i_D = 0$ mA

Fig.2.21. Equivalent schematics for a) *D – on*, b) *D – off.*

Steps 3 and 4.
Replace the values for i_D and v_D in the circuit's equations, found at Step 1.
D - on

$$-\ v_I - 0.7 - i_D \cdot R = 0$$
$$-\ v_I - 0.7 + v_O = 0$$
$$\boldsymbol{v_O = v_I + 0.7}$$
$$v_O = -\ i_D \cdot R < 0$$
$$v_I + 0.7 < 0$$
$$\boldsymbol{v_I < -\ 0.7\ V}$$

D - off

$$\boldsymbol{v_O = -\ i_D \cdot R = 0}$$
$$v_O = v_I + v_D$$
$$v_D = v_O - v_I = -\ v_I$$
$$\boldsymbol{v_I > -\ 0.7\ V}$$

Step 5.
Plot the VTC $v_O(v_I)$ for $v_I \in$ [-10 V; 10 V] (Fig.2.22).

b) The circuit delivers only the negative half-wave of the input at the output. Hence, the application of the circuit is voltage limiter or voltage clamp.

c) The waveforms for $v_I(t)$ and $v_O(t)$ are in Fig.2.23 and Fig.2.24.

d) The current through the diode is positive when the diode is *on*. The expression of v_D and the range of values for v_I when the diode is *on* are:

$$v_O = v_I + 0.7$$
$$v_I < -\ 0.7\ V$$

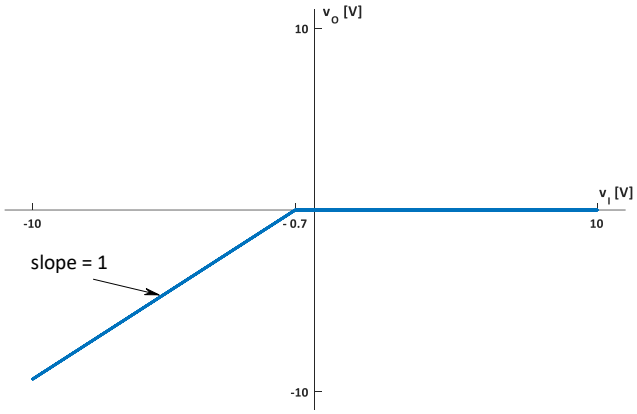


Fig.2.22. VTC $v_O(v_I)$

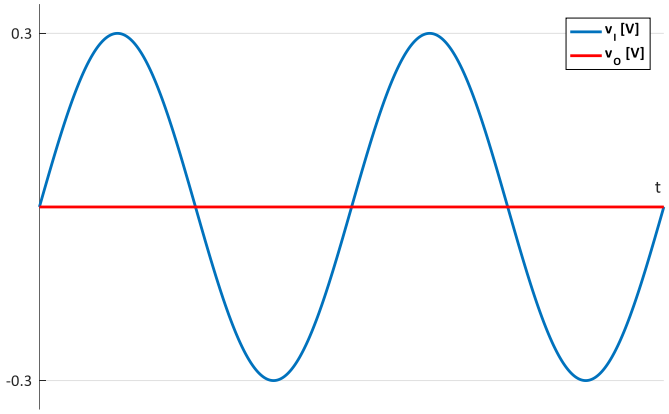


Fig.2.23. Waveforms of $v_I(t)$ and $v_O(t)$ for $v_I(t) = 0.3\sin\omega t$ [V]

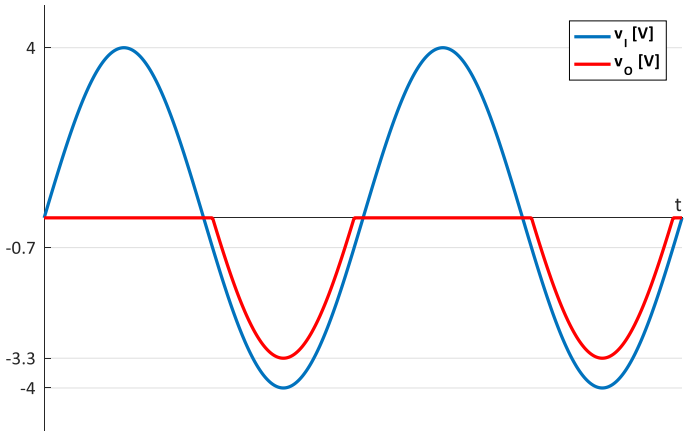


Fig.2.24. Waveforms of $v_I(t)$ and $v_O(t)$ for $v_I(t) = 4\sin\omega t$ [V]

By replacing in the expression of v_O, R is computed as:

$$v_O = -\ i_D \cdot R < 0$$

$$v_I + 0.7 = -\ i_D \cdot R$$

$$R = -\ \frac{v_I + 0.7}{i_D}$$

The maximum current through the diode is obtained for $v_{I\,min}$ = - 4 V.

$$R_{min} = - \frac{(-4 + 0{,}7)}{30 \cdot 10^{-3}}$$

$$R_{min} = 110\ \Omega$$

Thus, the range of values for R is [110 Ω; ∞).
The waveforms for $v_I(t)$, $v_O(t)$ and $i_D(t)$ are shown in Fig.2.25.

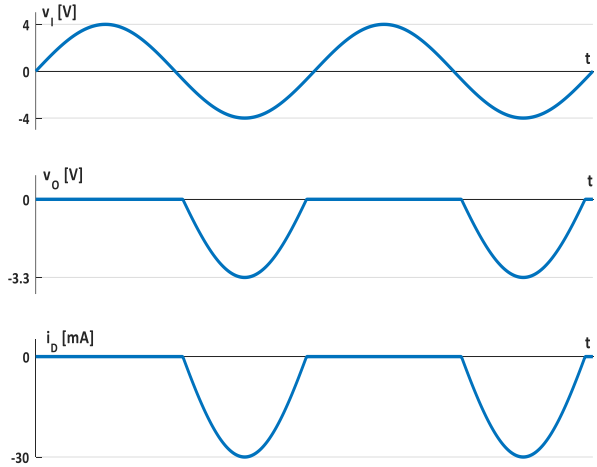


Fig.2.25. Waveforms for $v_I(t)$, $v_O(t)$ and $i_D(t)$ for $v_I(t) = 4\sin\omega t$ [V]

Another way of determining the VTC $v_O(v_I)$ for *DR* switching circuits is by computing the voltages in the anode and in the cathode of the diode. The voltage drop across the diode v_D is the difference between v_A and v_K (Fig.2.26).

$$v_D = v_A - v_K$$

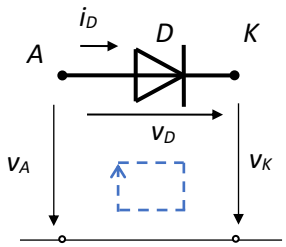


Fig.2.26. Voltage drop across the diode v_D expressed as the difference between v_A and v_K

Example

Deduce and plot the VTC $v_O(v_I)$ for the circuit in Fig.2.18. b).

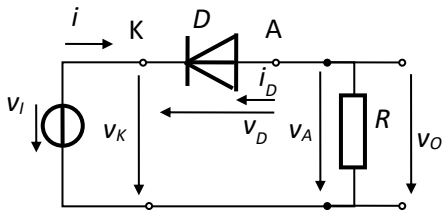
Solution:

The circuit in Fig.2.18. b) is shown once again, for convenience. The voltage drop across the diode v_D is the difference between v_A and v_K.

$$v_A = v_O = - i_D \cdot R$$

$$v_K = v_I$$

$$v_D = v_A - v_K = v_O - v_I$$



When the diode is *on*: $v_D = 0.7$ V and $i_D > 0$

$v_O - v_I = 0.7$ V

$\boldsymbol{v_O = v_I + 0.7}$

$v_O < 0$

$v_I + 0.7 < 0$

$\boldsymbol{v_I < -0.7}$ V

When the diode is *off*: $i_D = 0$ and $v_D < 0.7$

$v_O - v_I < 0.7$

$v_O - 0.7 < v_I$

$\boldsymbol{v_O = 0}$

$\boldsymbol{v_I > -0.7}$ V

The VTC is the one shown in Fig.2.22.

Problems

1. For the circuit in Fig.2.18. a), using the constant voltage drop model for the diode:
a) deduce and plot $v_O(v_I)$ for $v_I \in$ [-8 V; 8 V]
b) specify the application of the circuit
c) determine the minimum value of the input voltage for which the output voltage is not zero.

2. For the circuit in Fig.2.18. a), using the constant voltage drop model for the diode:
a) plot $v_I(t)$ and $v_O(t)$ for
i) $v_I(t) = 0.4\sin\omega t$ [V]
ii) $v_I(t) = 7\sin\omega t$ [V].
b) compute the maximum power dissipation on $R = 300\ \Omega$ for $v_I(t) = 7\sin\omega t$ [V].

3. For the circuit in Fig.2.18. c), using the constant voltage drop model for the diode:
a) deduce and plot $v_O(v_I)$ for $v_I \in$ [-12 V; 12 V]
b) specify the application of the circuit
c) plot $v_I(t)$ and $v_O(t)$ for $v_I(t) = 10\sin\omega t$ [V]
d) what is the range of values for R, if the maximum current through the diode is $I_{Dmax} = 45$ mA and $v_I(t) = 10\sin\omega t$ [V]?

4. For the circuit in Fig.2.18. d), using the constant voltage drop model for the diode:
a) deduce and plot $v_O(v_I)$ for $v_I \in$ [-12 V; 12 V]
b) specify the application of the circuit
c) plot $v_I(t)$ and $v_O(t)$ for
i) $v_I(t) = 0.5\sin\omega t$ [V]
ii) $v_I(t) = 0.9\sin\omega t$ [V]
iii) $v_I(t) = 9\sin\omega t$ [V]
d) what is the range of values for R, if the maximum power dissipation on the diode is $P_{Dmax} = 35$ mW

and $v_I(t) = 9\sin\omega t$ [V]?
e) compute the power dissipation on the diode, for the values determined at d).

Connecting the diode in parallel with the voltage source and the resistor is not recommended (Fig.2.27. a). When the diode is *on*, two voltage sources (v_I and v_D) appear in parallel in the equivalent circuit (Fig.2.27. b). This determines a theoretically infinite current through the circuit, which is destructive.

If the diode and the resistor must be connected in parallel, the circuit needs to be supplied with a current source instead of a voltage source, thus preventing the destruction of the diode.

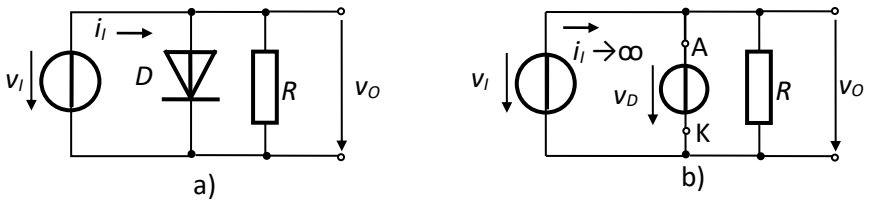


Fig.2.27. *DR* circuit, parallel connection – **to be avoided**
a) circuit; b) equivalent circuit for *D* – *on.*

2.3.3 Analysis of *DR* switching multi-port circuits

A *DR* switching circuit with more than two ports is called a multi-port. *DR* switching two-port circuit is a particular case of multi-port. Usually, a multi-port circuit has multiple inputs and one output.

The analysis of *DR* switching multi-port circuits uses the same method as the analysis of *DR* switching two-port circuits, namely:
– write the circuit's equations, using Ohm's law, Kirchhoff's voltage law and Kirchhoff's current law
– draw the equivalent schematics for the *on* and *off* states of the diodes, using the constant voltage drop model
– customize the circuit's equations for each state of the diodes, by using the values of v_D and i_D from the constant voltage drop model
– find v_O and the range of values for v_I, for the *on* and *off* states of the diodes. Write the complete expression of $v_O(v_I)$.

DR multi-port circuits where the diodes share a common terminal (either anode or cathode) are analysed next.

The maximum three-port circuit consists of two diodes and a resistor (Fig. 2.28). The two diodes have their cathodes connected.

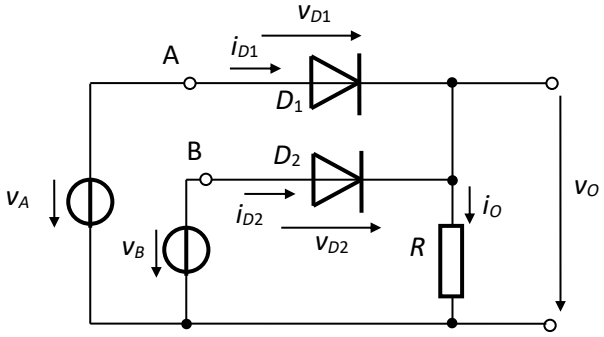


Fig.2.28. Maximum three-port circuit

The graphical representation of the output voltage as a function of the two input voltages is a three-dimensional plot. This 3D plot can be simplified to a two-dimensional family of characteristics, by assuming one of the input voltages is constant. For this type of circuits, the electrical function will be deduced and the waveforms of the input and output voltages, with respect to time, will be plotted.

Assuming the clockwise direction for all circuit loops, the equations of the circuit are:

$$v_{D1} + v_O - v_A = 0$$
$$v_{D2} + v_O - v_B = 0$$
$$v_{D1} - v_{D2} + v_B - v_A = 0$$
$$i_{D1} + i_{D2} = i_O$$
$$v_O = i_O \cdot R$$

For the three-port circuit in Fig.2.28, there are four equivalent schematics to analyse, based on the states of the two diodes: both diodes *on*, both diodes *off*, first diode *on* and second diode *off*, first diode *off* and second diode *on.*

Equivalent schematic 1 – when both diodes are *off*, the equivalent schematic is shown in Fig.2.29. The output voltage is zero.

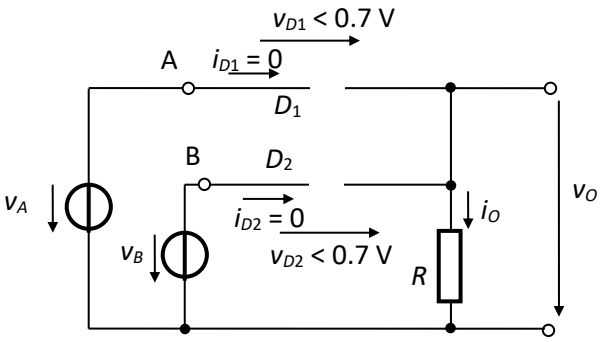


Fig.2.29. Equivalent circuit – D_1 and D_2 *off*

$$\boldsymbol{v_O = 0\ V}$$
$$i_O = 0\ \text{mA}$$
$$v_{D1} = v_A - v_O = v_A$$
$$v_{D2} = v_B - v_O = v_B$$
$$\boldsymbol{v_A < 0.7\ V}$$
$$\boldsymbol{v_B < 0.7\ V}$$

When one diode is *on* and the other one is *off*, the equivalent circuit is identical to the one in Fig.2.18. a). For D_1 - *on* and D_2 – *off*, the output voltage only depends on v_A.

$$\boldsymbol{v_O = v_A - 0.7\ V}$$
$$i_{D2} = 0\ \text{mA}$$
$$v_O = i_{D1} \cdot R$$
$$\boldsymbol{v_A > 0.7\ V}$$
$$v_{D2} = v_B - v_A + 0.7 < 0.7$$
$$\boldsymbol{v_A > v_B}$$

For D_1 - *off* and D_2 – *on*, the output voltage only depends on v_B.

$$\boldsymbol{v_O = v_B - 0.7\ V}$$

$$i_{D1} = 0 \text{ mA}$$
$$v_O = i_{D2} \cdot R$$
$$\boldsymbol{v_B > 0.7 \text{ V}}$$
$$v_{D2} = v_B - v_A + 0.7 < 0.7$$
$$\boldsymbol{v_B > v_A}$$

To have both diodes *on*, the two input voltages must be equal at the same time, and the two diodes must have the same threshold voltage. Such a perfect match is rarely achievable in practical circuits. In theory, if both diodes are *on*, the equations are:

$$v_A = v_B = v_I$$
$$\boldsymbol{v_O = v_I - 0.7 \text{ V}}$$
$$v_O = (i_{D1} + i_{D2}) \cdot R$$
$$i_O = i_{D1} + i_{D2}$$
$$\boldsymbol{v_I > 0.7 \text{ V}}$$

By analysing the expressions of the output voltage for each of the four equivalent circuits, the final output voltage is computed as:

$$v_O = \max (v_A - 0.7; v_B - 0.7; 0 \text{ V})$$

Since the input voltages are variable in time, the application of the circuit - *spatial maximum circuit* - becomes obvious: the output voltage is the maximum between the input voltages, at any moment of time.

$$v_O(t) = \max (v_A(t) - 0.7; v_B(t) - 0.7; 0 \text{ V})$$

For the circuit in Fig.2.29, the output voltage is always positive, with a minimum value of 0 V. If a new minimum value of the output voltage is desired, an additional dc voltage source (positive or negative) must be added in the circuit, as shown in Fig.2.30. The output voltage of the circuit also depends on the newly added voltage source, V_C.

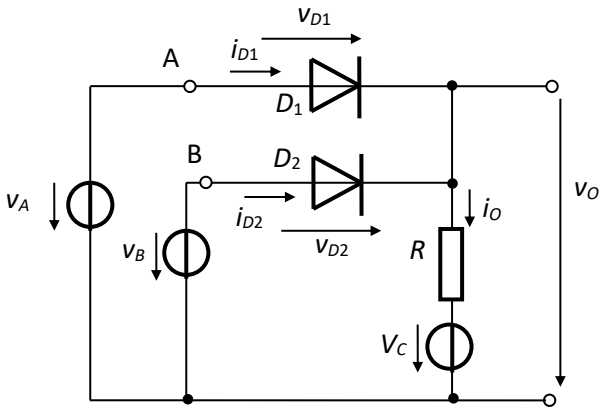


Fig.2.30. Spatial maximum multi-port circuit with $V_{Omin} = V_C$

The output voltage expressed using KVL is:

$$v_O = i_O \cdot R + V_C$$

When both diodes are *off*, there are no currents through the circuit, and the output voltage is equal to V_C. Both diodes are *off* if the voltage in their anode is less than (V_C + 0.7 V).

The final expression of the output voltage is:

$$v_O = \max (v_A - 0.7; v_B - 0.7; V_C)$$

DR multi-port circuits with more than two inputs can be built, and the above expression can be

generalized.

When analysing a DR two-port circuit, the above expression can be customized. If the circuit in Fig.2.18. a) is seen as a spatial maximum circuit with one input, the output voltage is written as:

$$v_O = \max (v_I - 0.7;\ 0\ \text{V})$$

Examples

1. Determine the expression of the output voltage and plot $v_1(t)$, $v_2(t)$, $v_O(t)$ and $i_O(t)$ for the circuit in Fig.2.28, if:

- R = 4 kΩ
- $v_1(t)$ – rectangular signal, 5 V amplitude and 50 Hz frequency
- $v_2(t)$ – sinusoidal signal, 8 V amplitude and 100 Hz frequency.

Solution:

The output voltage and the output current are:

$$v_O = max\,(v_1(t) - 0.7;\ v_2(t) - 0.7;\ 0\ \text{V})$$

$$i_O(t) = \frac{v_O(t)}{R}$$

The waveforms for $v_1(t)$, $v_2(t)$, $v_O(t)$ and $i_O(t)$ are depicted in Fig.2.31.

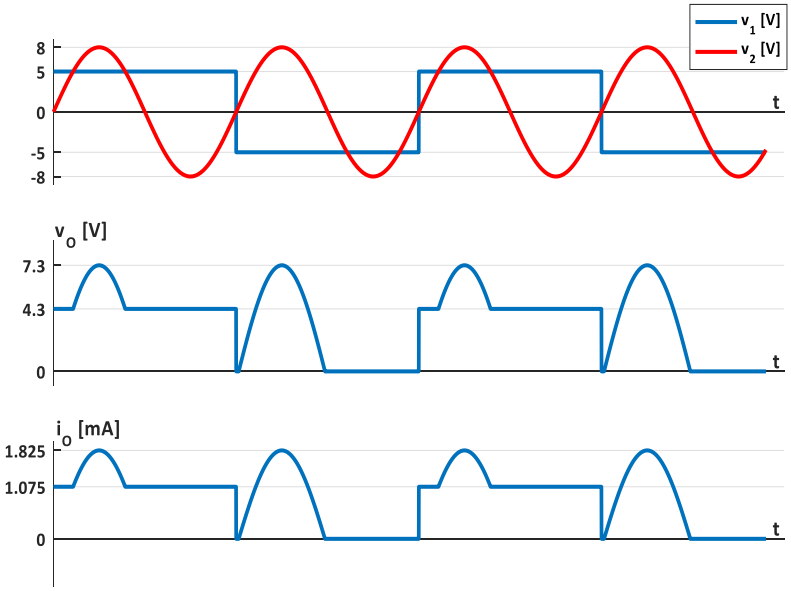


Fig.2.31. Waveforms for $v_1(t)$, $v_2(t)$, $v_O(t)$ and $i_O(t)$

2. Compute the values of v_O, v_{D1}, v_{D2}, i_{D1}, i_{D2}, i_O for the circuit in Fig.2.30, if V_A = 6 V, V_B = 2 V, V_C = -9 V and R = 2 kΩ. Assume the constant voltage drop model for the diodes.

Solution:

The output voltage is:

$$v_O = \max (6 - 0.7;\ 2 - 0.7;\ -9) = \max (5.3;\ 1.3;\ -9) = 5.3\ \text{V}$$

Diode D_1 is *on*, diode D_2 is *off*. The values for v_{D1} and i_{D2} are determined from the diode's equations:

$$v_{D1} = 0.7\ \text{V}$$

$$i_{D2} = 0\ \text{mA}$$

$$i_O = i_{D1} + i_{D2} = i_{D1}$$
$$i_O = \frac{v_O}{R}$$
$$i_O = \frac{5.3}{2 \cdot 10^3} = 2{,}65 \text{ mA}$$
$$i_{D1} = i_O = 2.65 \text{ mA}$$
$$v_{D2} = v_B - v_O$$
$$v_{D2} = 2 - 5.3 = -3.3 \text{ V}$$

The value of i_{D1} must be positive, and the value of v_{D2} must be below 0.7 V.

The minimum three-port circuit is obtained by connecting the anodes of the diodes in a common point, while the input voltages are applied in the cathodes of the diodes, as shown in Fig.2.32.

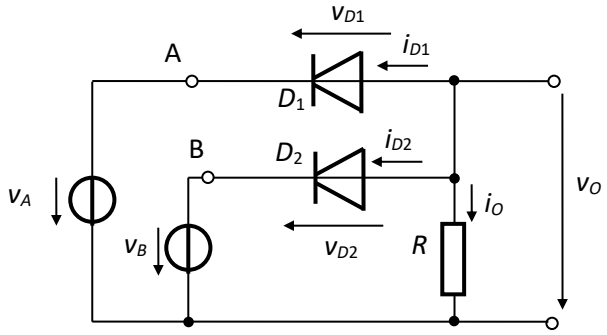


Fig.2.32. Minimum three-port circuit

The equations of the circuit, considering the clockwise direction, are:

$$-v_{D1} + v_O - v_A = 0$$
$$-v_{D2} + v_O - v_B = 0$$
$$-v_{D1} + v_{D2} + v_B - v_A = 0$$
$$i_{D1} + i_{D2} = i_O$$
$$v_O = i_O \cdot R$$

By using the values of i_D and v_D for the *on/off* states of the diodes in all four equivalent circuits, the electrical function of the circuit is spatial minimum.

$$v_O = \min (v_A + 0.7; v_B + 0.7; 0 \text{ V})$$

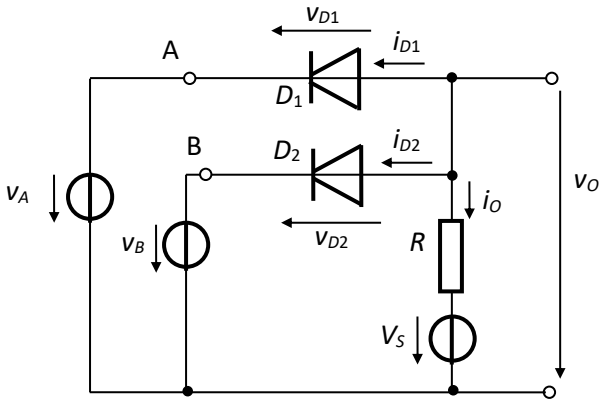


Fig.2.33. Spatial minimum multi-port circuit with $V_{Omax} = V_S$

The maximum value of the output voltage is 0 V. To obtain positive output voltages, an additional positive dc voltage source must be added in the circuit, as shown in Fig.2.33.

Usually, the value of this source is the maximum value of the two input voltages. The output voltage of the circuit also depends on the newly added voltage source, V_S.

$$v_O(t) = min\ (v_A(t) + 0.7;\ v_B(t) + 0.7;\ V_S)$$

Example

Plot $v_A(t)$, $v_B(t)$ and $v_O(t)$ for the circuit in Fig.2.33, if:
- R = 8 kΩ
- $v_A(t)$ - rectangular signal, 4.7 V amplitude and 20 Hz
- $v_B(t)$ – triangular signal, 8 V amplitude and 50 Hz frequency
- V_S = 8 V.

Solution:

The circuit is a spatial minimum circuit, so the output voltage is

$$v_O(t) = \min\ (v_A(t) + 0.7;\ v_B(t) + 0.7;\ 8)$$

The output current is $i_O(t) = \frac{v_O(t)}{R}$

The waveforms for $v_A(t)$, $v_B(t)$ and $v_O(t)$ are shown in Fig.2.34.

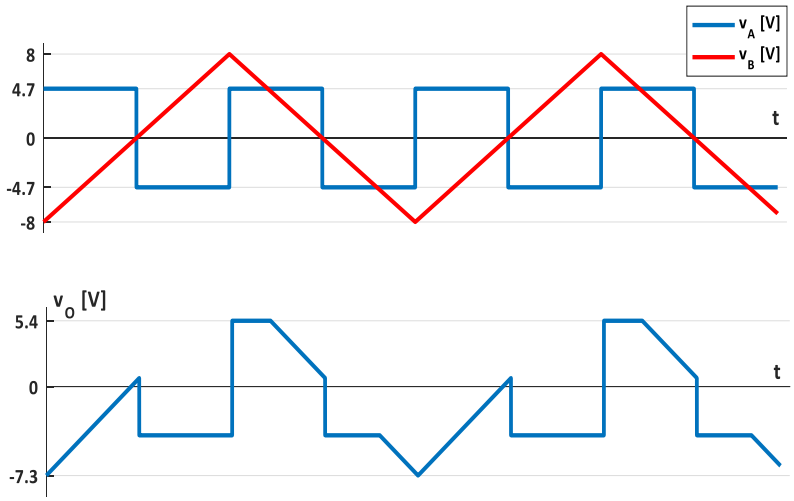


Fig.2.34. Waveforms for $v_A(t)$, $v_B(t)$ and $v_O(t)$

Problems

1. Determine the expression of the output voltage and plot $v_1(t)$, $v_2(t)$, $v_O(t)$ and $i_O(t)$ for the circuit in Fig.2.28, if R = 2.5 kΩ, $v_1(t)$ – sinusoidal, 7.7 V amplitude, 50 Hz frequency, and V_2 = 5.7 V.

2. Determine the expression of the output voltage and plot $v_1(t)$, $v_2(t)$, $v_O(t)$ and $i_O(t)$ for the circuit in Fig.2.28, if R = 5 kΩ, $v_1(t) = 10\sin\omega t$ [V] and $v_2(t) = -v_I(t)$. What is the application of the circuit (other than spatial maximum), for the given input voltages?

3. Compute the values for v_O, v_{D1}, v_{D2}, i_{D1}, i_{D2}, i_O for the circuit in Fig.2.28, if V_A = -7 V, V_B = -2 V and R = 2 kΩ. Assume the constant voltage drop model for the diodes.

4. Compute the values for v_O, v_{D1}, v_{D2}, i_{D1}, i_{D2}, i_O for the circuit in Fig.2.30, if V_A = -7 V, V_B = -2 V, V_C = -10 V and R = 2 kΩ. Assume the constant voltage drop model for the diodes.

5. Determine the expression of the output voltage and plot $v_1(t)$, $v_2(t)$, $v_O(t)$ and $i_O(t)$ for the circuit in Fig.2.30, if R = 5 kΩ, $v_I(t) = 10\sin\omega t$ [V], $v_2(t)$ – rectangular voltage, 5 V amplitude, same frequency as $v_I(t)$, and V_C = - 3 V.

6. Determine the expression of the output voltage and plot $v_A(t)$, $v_B(t)$ and $v_O(t)$ for the circuit in Fig.2.30, if R = 4 kΩ, $v_A(t)$ is sinusoidal, 8 V amplitude and 25 Hz frequency, $v_B(t)$ is rectangular, 5V amplitude and twice the frequency of $v_A(t)$, and V_C = - 3 V. Find the minimum value of R if the maximum current allowed through each diode is I_{Dmax} = 120 mA.

7. Compute the values for v_O, v_{D1}, v_{D2}, i_{D1}, i_{D2}, i_O for the circuit in Fig.2.32, if V_A = 6 V, V_B = 4 V, V_S = 10 V and R = 2 kΩ. Assume the constant voltage drop model for the diodes.

8 - 10. Problems **1**, **2**, **3** for the circuit in Fig.2.32.

11, 12. Problems **5**, **6** for the circuit in Fig.2.33.

2.3.4 Applications of *DR* switching circuits

The application of a *DR* switching circuit is given by the cases the circuit is used in. The same circuit can be analysed from various perspectives, thus the applications can be different. Such an example is a *DR* switching two-port circuit, that can be seen as a voltage limiter (clamp), but also as a spatial extreme circuit (minimum or maximum).

Simple voltage limiter (clamp)

Any of the four possible *DR* two-port circuits works as a voltage limiter. For the circuits where the output is measured across *R*, the output voltage is limited to 0 V. For the circuits where the output is measured across *D*, the output voltage is limited to either +0.7 V or -0.7 V, depending on the orientation of the diode.

When the output voltage needs to be limited to values other than ±0.7 V, the most common solution is to connect multiple diodes, in series, with the same orientation. This way, the output voltage is now limited to multiples ±0.7 V. For the circuit in Fig.2.35. a), the maximum output is 2.1 V, while for the circuit in Fig.2.35. b), the minimum input is -1.4 V.

The VTCs still show two segments since all diodes have the same state at the same time (both *on* or both *off*) (Fig.2.36 a) and b). A drawback of using multiple diodes in series in real circuits is than the voltage drop across the diode in *on* state depends on the current through the diode, and is not a constant value of 0.7 V.

To deduce the VTC $v_O(v_I)$ for the circuits in Fig.2.35, the steps are identical to the ones used to analyse *DR* switching two-port circuits: write the circuit's equations and customize them for all possible equivalent circuits.

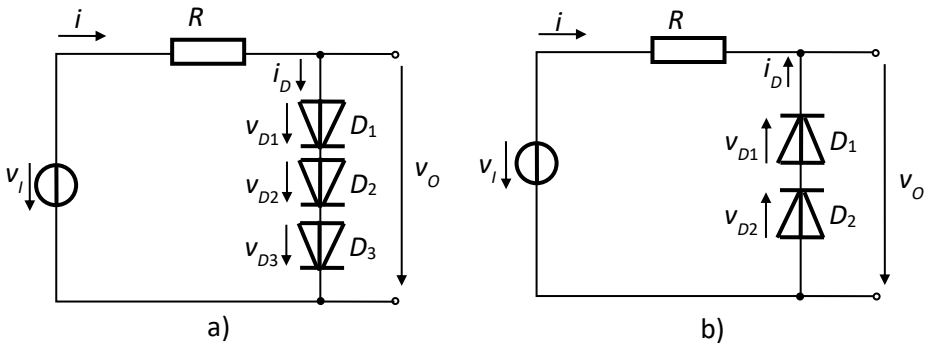


Fig.2.35 Voltage limiters with multiple diodes in series
a) superior, V_{Omax} = 2.1 V, b) inferior, V_{Omin} = -1.4 V.

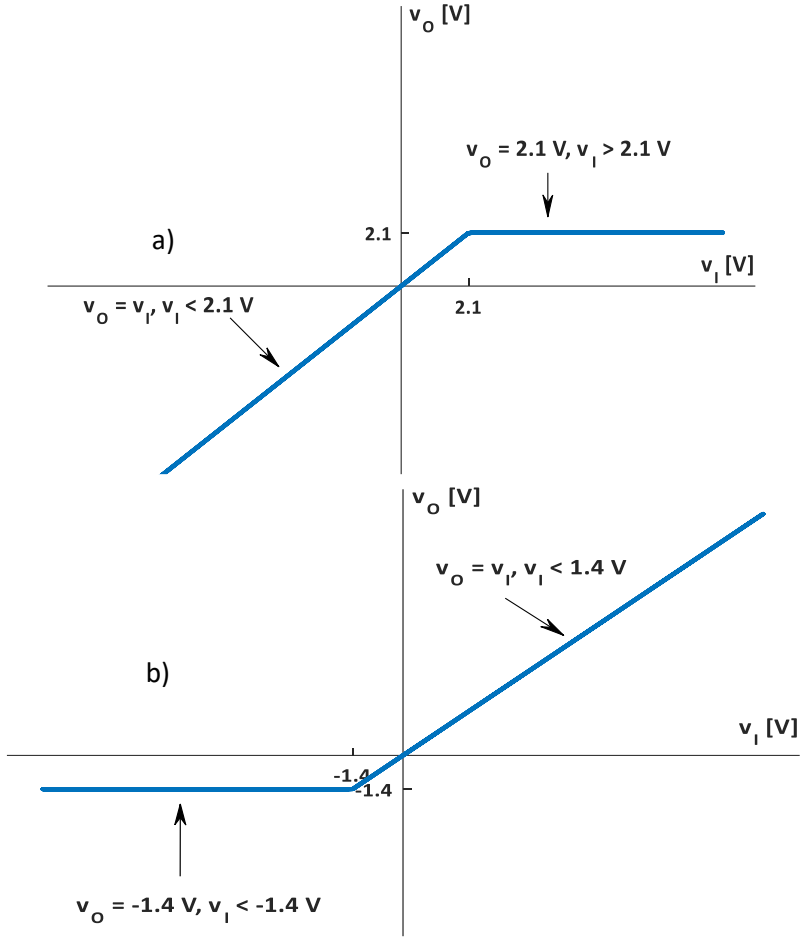


Fig.2.36. VTC $v_O(v_I)$ for the circuits in Fig.2.35.
a) V_{Omax} = 2.1 V, b) V_{Omin} = -1.4 V.

Another method of obtaining a different limit for the output voltage (other than ±0.7 V) is to connect a dc voltage source V_{BIAS} (positive or negative), in series with the element the output voltage is measured across. In practical cases, V_{BIAS} can be obtained from regular diodes (as previously explained) or from Zener diodes (to be discussed in another section).

All four *DR* two-port circuits in Fig.2.18 can be upgraded to versions that limit the output voltage to values different from 0 V or ±0.7 V, as shown in Fig.2.37.

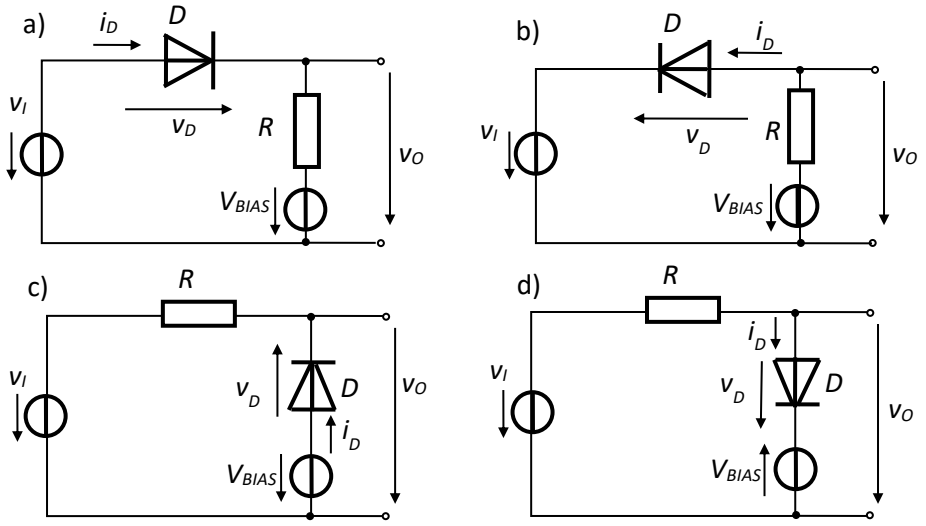


Fig.2.37. *DR* voltage limiters with V_{BIAS}
a) inferior, $V_{Omin} = V_{BIAS}$; b) superior, $V_{Omax} = V_{BIAS}$;
c) inferior, $V_{Omin} = V_{BIAS} - 0.7$ V; d) superior, $V_{Omin} = -V_{BIAS} + 0.7$ V.

The equations of the circuit in Fig.2.37. a) and the equations for the two segments of the VTC are:

$$v_I = v_D + v_O$$
$$v_O = i_D \cdot R + \boldsymbol{V_{BIAS}}$$
$$v_I = v_D + i_D \cdot R + \boldsymbol{V_{BIAS}}$$

Table 2.1. Equations for the two segments of the VTC for the circuit in Fig.2.37. a)

D - on	***D - off***
$v_O = v_I - 0.7$	$v_O = V_{BIAS}$
$v_I > 0.7 + V_{BIAS}$	$v_I < 0.7 + V_{BIAS}$

The VTC $v_O(v_I)$ is shown in Fig.2.38, where the red dotted line represents the VTC $v_O(v_I)$ for the circuit without V_{BIAS}.

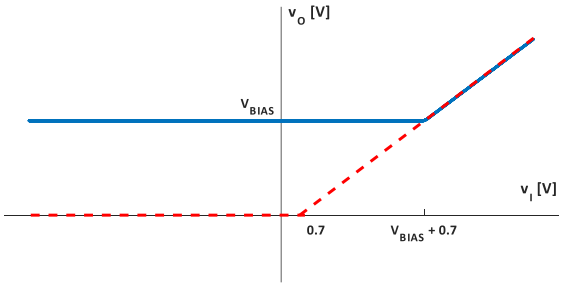


Fig.2.38. VTC $v_O(v_I)$ for the inferior voltage limiter in Fig.2.37. a)

Examples	
1. Design a superior voltage limiter, with $V_{Omax} = 1.4$ V, and compute the minimum value of R for which the current through the diode doesn't exceed $I_{Dmax} = 150$ mA, for $v_I(t) = 7.4\sin\omega t$ [V].	

Solution:

Two possible superior voltage limiters are shown in Fig.2.39.

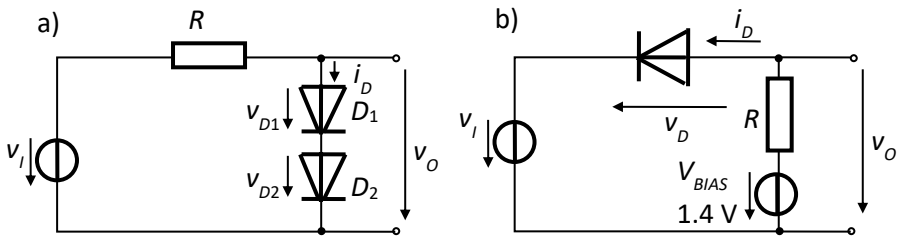


Fig.2.39. Superior voltage limiter, V_{Omax} = 1.4 V
a) output measured across diodes; b) output measured across R and V_{BIAS}.

For the circuit in Fig.2.39. a), the diodes are *on* when $v_I > 1.4$ V, so $V_O = 1.4$ V. For any $v_I < 1.4$ V, the diodes are *off*, and $v_O = v_I$. The current through the diodes exists only when both diodes are *on*, meaning when $V_O = 1.4$ V.

$$i_D \cdot R = v_I - v_O$$

$$R_{min} = \frac{v_I - v_O}{I_{Dmax}}$$

$$R_{min} = \frac{7.4 - 1.4}{150 \cdot 10^{-3}} = 40\ \Omega$$

For the circuit in Fig.2.39. b), the diode is *on* when $v_I < 0.7$ V (the voltage in the anode is already 1.4 V).

$$v_O = v_I + v_D = v_I + 0.7\ \text{V}$$

The diode is *off* when $v_I > 0.7$ V, for which $V_O = 1.4$ V. The value of R is computed as:

$$-v_D - i_D \cdot R + V_{BIAS} - v_I = 0$$

$$i_D \cdot R = -0.7 + 1.4 - v_I = 0.7 - v_I$$

$$R_{min} = \frac{0.7 - v_I}{I_{Dmax}}$$

$$R_{min} = \frac{0.7 - (-7.4)}{150 \cdot 10^{-3}} = 54\ \Omega$$

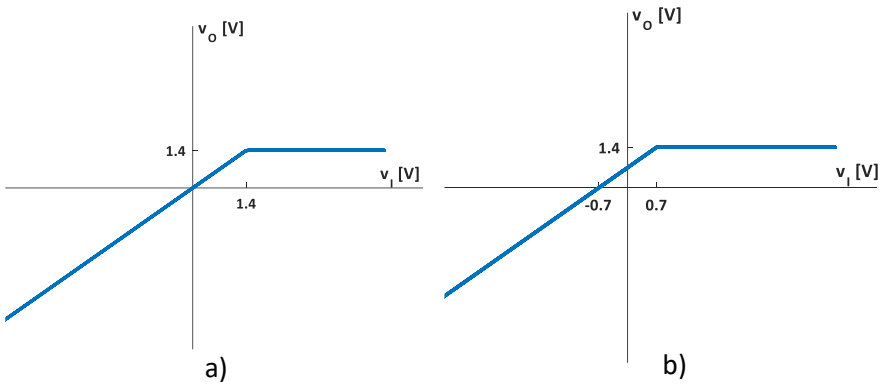


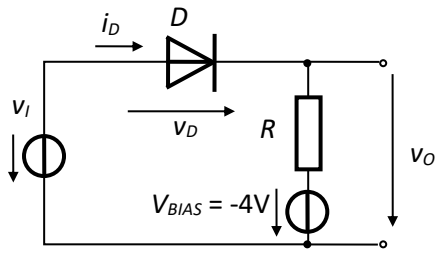
Fig.2.40. VTCs $v_O(v_I)$ for the circuits in
a) Fig.2.39. a); b) Fig.2.39. b).

Two different values for the resistor are thus obtained. Even if both circuits limit the output voltage to 1.4 V, the VTCs $v_O(v_I)$ are different, as seen in Fig.2.40. For the first circuit, the plot goes through the origin.

2. Design an inferior voltage limiter, with V_{Omin} = -4 V. Show that the circuit is an inferior voltage limiter and plot $v_I(t)$ and $v_O(t)$ for $v_I(t) = 9\sin\omega t$ [V].

Solution:

The limit value of the output voltage is not a multiple of 0.7 V, which means that the limit is given by an additional dc voltage source, V_{BIAS}, connected so that it is included in the output voltage, as shown in Fig.2.37. a) and once again below.



To prove that the circuit is an inferior voltage limiter, the circuit's equations are written and then customized for *on* and *off* states of the diode.

$$v_O = v_I - v_D$$
$$v_O = i_D \cdot R + V_{BIAS} = i_D \cdot R - 4\ \text{V}$$

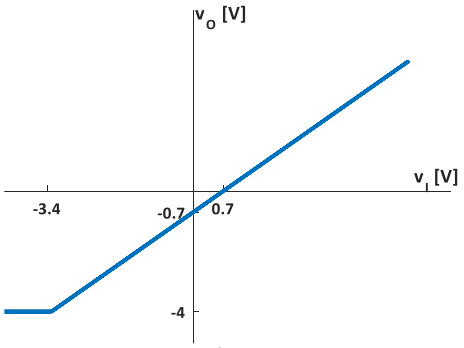
When *D - on*

$$v_O = v_I - 0.7\ \text{V}$$
$$v_I > -3.3\ \text{V}$$

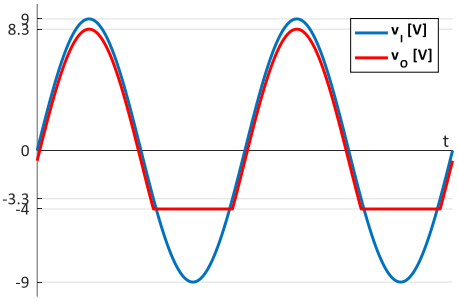
When *D - off*

$$v_O = -4\ \text{V}$$
$$v_I < -3.3\ \text{V}$$

The minimum output voltage is -4 V. The VTC $v_O(v_I)$ is shown in Fig.2.41. a), and the waveforms for the input and output voltages are Fig.2.41. b).



a)



b)

Fig.2.41. Inferior voltage limiter
a) VTC $v_O(v_I)$; b) waveforms.

Double voltage limiter

The circuits analysed up this point limit the output voltage to either an inferior or a superior value. A double voltage limiter imposes both an inferior limit, V_{Omin}, and a superior limit, V_{Omax}. The easiest way to achieve double voltage limitation is by using two diodes, connected in antiparallel (opposite parallel), as shown in Fig.2.42.

Diodes will never be *on* at the same time, because of their orientation in the circuit. Diode D_1 is *on* for an input voltage greater than 0.7 V, while diode D_2 is *on* for an input voltage smaller than -0.7 V.

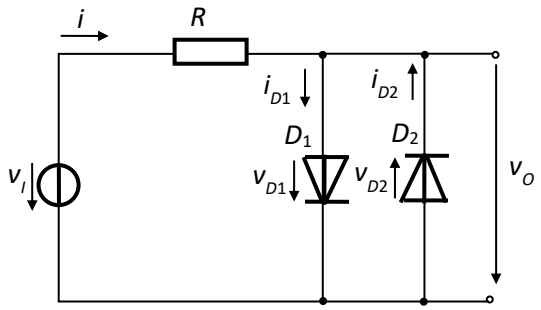


Fig.2.42. Double voltage limiter, to 0.7 V and -0.7 V

D_1 - *on*, D_2 - *off*:

$$v_O = v_{D1} = 0.7 \text{ V}$$
$$v_I > 0.7 \text{ V}$$

D_2 - *on*, D_1 - *off*:

$$v_O = - v_{D2} = - 0.7 \text{ V}$$
$$v_I < - 0.7 \text{ V}$$

D_1 - *off*, D_2 - *off*:

$$v_O = v_I$$
$$- 0.7 \text{ V} < v_I < 0.7 \text{ V}$$

The VTC $v_O(v_I)$ is shown in Fig.2.43. a), and sample waveforms are depicted in Fig.2.43. b).

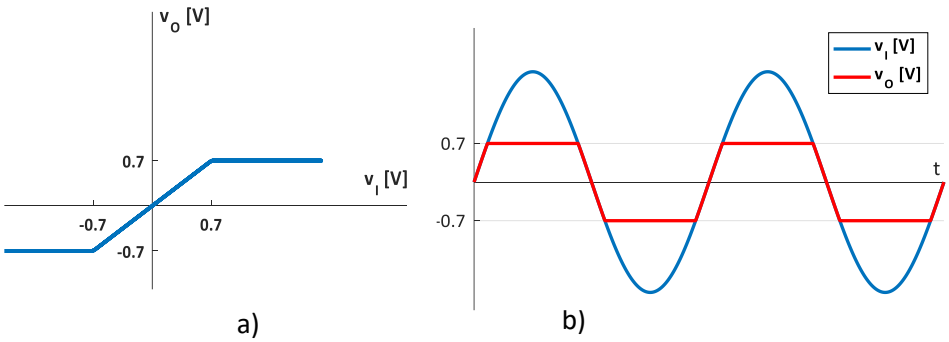


Fig.2.43. Double voltage limiter a) VTC $v_O(v_I)$; b) waveforms.

When the output voltage needs to be limited to values other than ±0.7 V, additional dc voltage sources (V_{BIAS1} and V_{BIAS2}) will be connected in series with the two diodes, as shown in Fig.2.44.

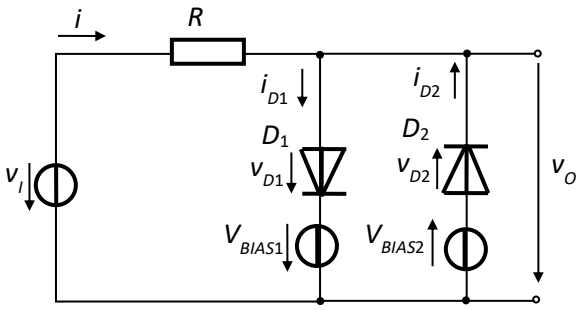


Fig.2.44. Double voltage limiter
$V_{Omax} = V_{BIAS1} + 0.7$ V and $V_{Omin} = -V_{BIAS2} - 0.7$ V

The dc voltage sources can be both positive, both negative, or one positive and the other negative. The only restriction regarding V_{BIAS1} and V_{BIAS2} is set by the relation between the limits of the output voltage: the superior limit must always be greater than the inferior limit. If this condition is not met, the circuit no longer works as a double voltage limiter.

Pulses selector

If the input voltage is a sequence of alternating positive and negative pulses, and only the positive pulses need to be selected at the output, a *DR* circuit with the output measured across the resistor (Fig.2.45) will do the trick. By flipping the diode, the negative pulses are delivered at the output.

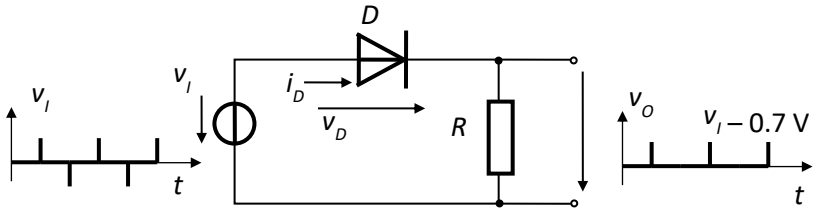


Fig.2.45. Positive pulses selector circuit

Half-wave rectifier

The *DR* circuit in Fig.2.45 is said to be a half-wave rectifier when the input signal is obtained from the secondary winding of a transformer. A half-wave rectifier delivers one half-wave (positive or negative) of the input signal at the output. The voltage obtained from the electrical outlet is 230 V effective value, and this voltage is connected to the primary winding of the transformer. If the transformer ratio is 23:1, the amplitude of the voltage in the secondary is 14.1 V.

$$\widehat{V_I} = \frac{230\sqrt{2}}{23} = 14.1 \text{ V}$$

The waveforms for the input and output voltages are shown in Fig.2.46.

Full-wave rectifier

A full-wave rectifier delivers both half-waves of the input voltage at the output, but the output is only positive (most common) or only negative. There are many circuits that can perform this task, and these circuits are found in systems where the ac signal needs to be transformed into dc signal.

The spatial maximum *DR* multiport acts as a full-wave rectifier when the two input voltages have a phase shift of 180^o (half a period). In practical implementations, the two input voltages v_I and $-v_I$ are

obtained from the secondary winding of a centre-tapped transformer, as shown in Fig.2.47. a). The waveforms are depicted in Fig.2.47. b). The voltage drop across the diode in *on* state can be neglected if the amplitude of the input signal is significantly bigger (e.g., 100 V).

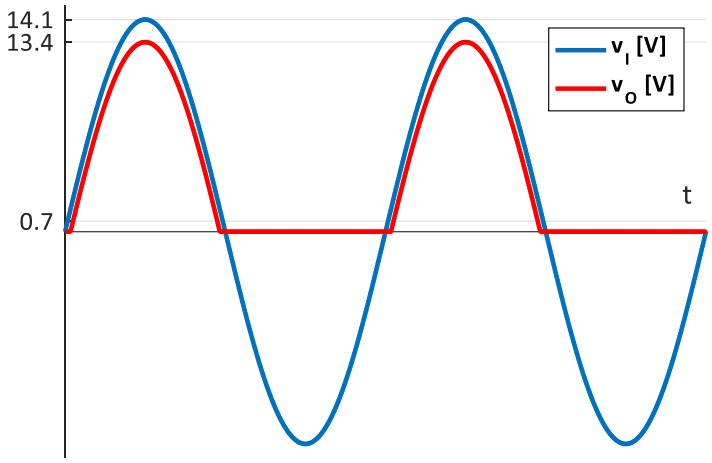


Fig.2.46. Half-wave rectifier - waveforms

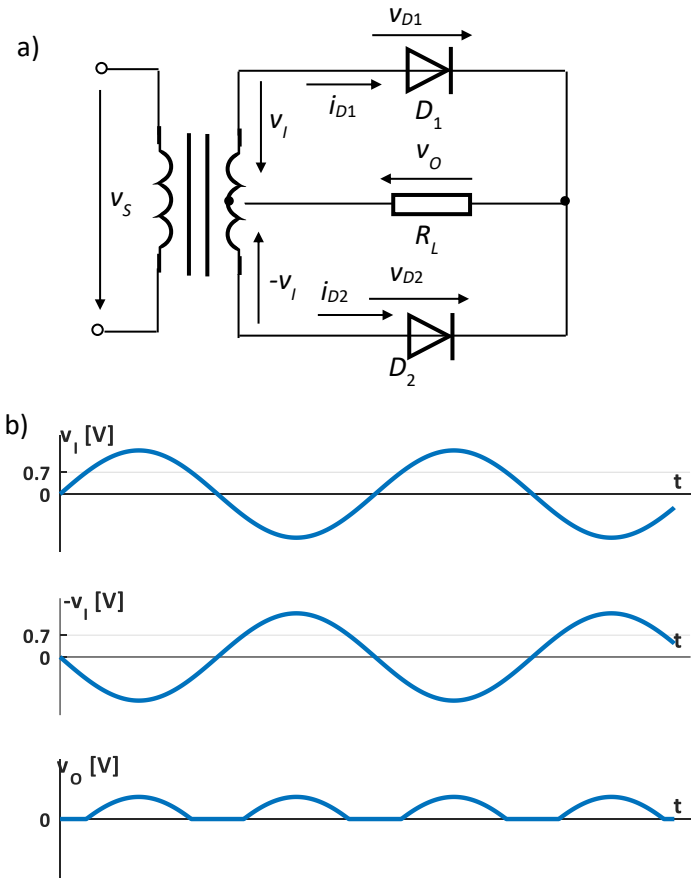


Fig.2.47. Full-wave rectifier obtained with a DR spatial maximum multi-port
a) circuit; b) waveforms.

Another version of a full-wave rectifier is the circuit in Fig.2.48, with the four diodes connected in

a diode bridge or rectifying bridge. The diodes are *on/off* based on the input voltage.

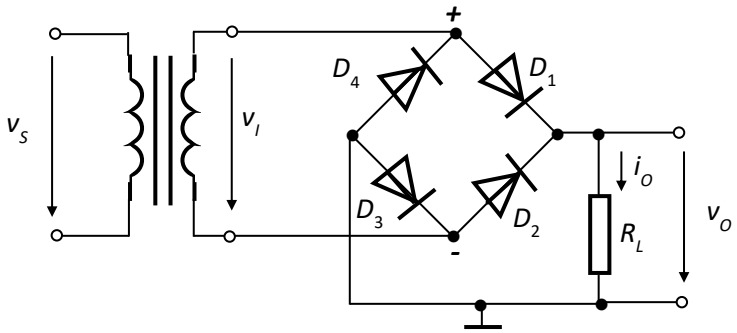


Fig.2.48. Full-wave diode brigde rectifier

Diodes D_1 and D_3 are *on* for $v_I > 1.4$ V, so $v_O = v_I - 1.4$ V. For this range of values of v_I, diodes D_2 and D_4 are *off*. The output current i_O is positive, meaning the output voltage is also positive.

Diodes D_2 and D_4 are *on* for $v_I < -1.4$ V, so $v_O = -v_I + 1.4$ V For this range of values of v_I, diodes D_1 and D_3 are *off*. The output current i_O is once again positive, meaning the output voltage is positive.

All four diodes are *off*, as long as $-1.4 \text{ V} < v_I < 1.4$ V. Here, both the output current and the output voltage are null.

The waveforms for the input and output voltages are shown in Fig.2.49.

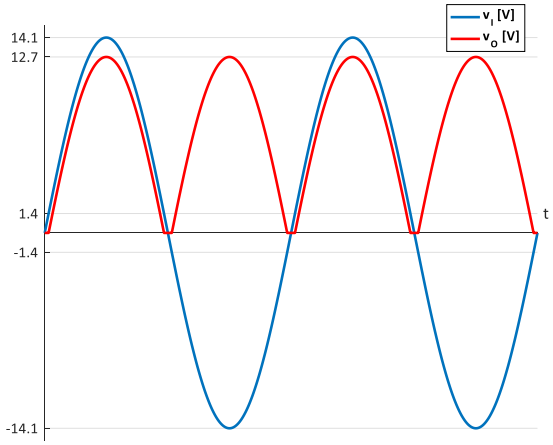


Fig.2.49. Waveforms for the full-wave diode bridge rectifier

Logic circuits

Logic circuits built with *DR* multi-ports are often the starting point when learning digital circuits. However, logic circuits built with *DR* multi-ports are not found in integrated circuits, where rapid switches between *on* and *off* are required.

To describe the behaviour of a logic circuit, two tables can be drawn: the *electrical operating table*, containing voltages and values in volts, and the *logic operating table or truth table*, containing logic variables and logic values, namely ”0” and ”1”.

A *DR* multi-port can implement the OR logic function (spatial maximum multi-port) and the AND logic function (spatial minimum multi-port). The number of inputs of the logic function is given by the number of input voltages.

A three inputs OR logic circuit, built with a spatial maximum multi-port, is shown in Fig.2.50.

The electrical operating table (Table 2.2) contains all eight combinations of values of the three input voltages. The truth table (Table 2.3) is obtained from the electrical operating table, by replacing the voltages with logic variables, and the values with logic values. The logic convention used here is 0

V – ”0” logic, 5 V – ”1” logic. The output voltage of 4.3 V is considered ”1” logic.

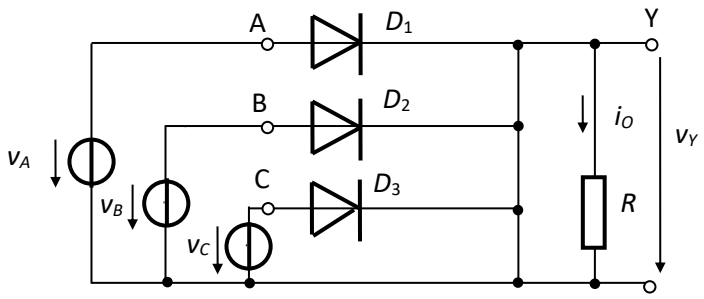


Fig.2.50. Three input OR logic circuit

Table 2.2. Electrical operating table

v_A [V]	V_B [V]	V_C [V]	V_Y [V]
0	0	0	0
0	0	5	4.3
0	5	0	4.3
0	5	5	4.3
5	0	0	4.3
5	0	5	4.3
5	5	0	4.3
5	5	5	4.3

Table 2.3. Truth table

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

The logic function of the circuit is deduced by analysing the truth table, and it can be written as a logic expression:

$$Y = A + B + C$$

For a logic AND circuit, an additional dc voltage source is connected in the anode of the diodes (Fig.2.33). The value of this voltage source must be equal to the value corresponding to”1” logic.

Problems

1. Design an inferior voltage limiter, with V_{Omin} = -1.4 V. Deduce and plot the VTC $v_O(v_I)$. Plot $v_I(t)$, $v_O(t)$ and $i_O(t)$ for $v_I(t) = 11\sin\omega t$ [V] and R = 4 kΩ.

2. Design a superior voltage limiter, with V_{Omax} = 7 V. Deduce and plot the VTC $v_O(v_I)$. Plot $v_I(t)$, $v_O(t)$ and $i_O(t)$ for $v_I(t) = 14\sin\omega t$ [V] and R = 0.5 kΩ.

3. For the circuit designed at Problem **2**, deduce and plot VTC $v_O(v_I)$ if the diode is flipped. What is the application of the new circuit? Plot $v_I(t)$, $v_O(t)$ and $i_O(t)$ of the new circuit, for $v_I(t) = 14\sin\omega t$ [V] and R = 0.5 kΩ.

4. For the voltage limiter in Fig.2.43, cu V_{BIAS1} = 6.3 V, V_{BIAS2} = -3.3 V and R = 5 kΩ:
a) deduce and plot the VTC $v_O(v_I)$ for $v_I \in$ [-10 V; 10 V].
b) plot $v_I(t)$, $v_O(t)$ and $i_O(t)$ for $v_I(t) = 3\sin\omega t$ [V]
c) plot $v_I(t)$, $v_O(t)$ and $i_O(t)$ for $v_I(t) = 6\sin\omega t$ [V]
d) plot $v_I(t)$, $v_O(t)$ and $i_O(t)$ for $v_I(t) = 10\sin\omega t$ [V].

5. For the full-wave diode bridge rectifier in Fig.2.48 and $v_I(t) = 12\sin\omega t$ [V]:
a) deduce and plot the VTC $v_O(v_I)$ for $v_I \in$ [-12 V; 12 V]
b) plot $v_I(t)$ and $v_O(t)$
c) find the minimum value of R for which the maximum output current is I_{Omax} = 160 mA.

6. For the full-wave diode bridge rectifier in Fig.2.48 with $v_I(t) = 9\sin\omega t$ [V] and R = 0.4 kΩ:
a) deduce and plot the VTC $v_O(v_I)$ for $v_I \in$ [-9 V; 9 V]. Specify the states of the four diodes on the plot.
b) plot $v_I(t)$ and $v_O(t)$.
c) plot the currents through D_1, $i_{D1}(t)$, and through D_2, $i_{D2}(t)$.

7. Design a three input AND logic circuit, using diodes. Use the logic convention 0 V – "0" logic and 3.3 V – "1" logic. Show that the circuit achieves the desired logic function.

8. For the circuit in Fig.2.50, specify the states of the three diodes and compute the current through each diode, for all eight lines of the electrical operating table.

2.4 *DC* switching circuits

DC switching circuits consist of diodes and capacitors. Since the capacitor is equivalent to an open circuit for dc signals, the VTC $v_O(v_I)$ is not relevant. *DC* switching circuits are analysed using ac input voltages.

There are four different versions of the series *DC* circuit built with one diode and one capacitor, based on the orientation of the diode and the element that the output voltage is measured on.

The analysis of these simple series *DC* circuits begins by establishing some premises:

- initially, the capacitor is discharged ($v_C(0) = 0$ V)
- the capacitor charges when a current passes through it. If the positive direction of the current is assumed, the capacitor will charge to a positive voltage.
- the current through the circuit only exists when the diode is *on*, thus the capacitor charges when the diode is *on*
- once charged to the maximum value, the capacitor maintains a constant voltage (does not discharge).

2.4.1 *DC* switching circuits with the output on *C*

The two *DC* circuits with the output voltage measured across the capacitor are shown in Fig.2.51.

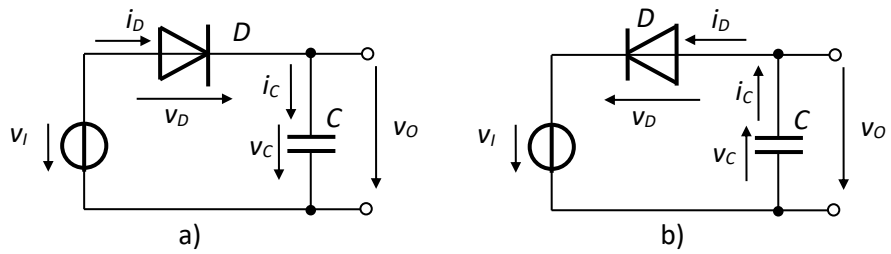


Fig.2.51. *DC* circuits, output on *C*
a) positive peak detector; b) negative peak detector.

The analysis is now detailed for the circuit in Fig.2.51. a). Initially, the capacitor is discharged:

$$v_C(0) = 0 \text{ V}$$

For the diode to be *on*, the input voltage needs to be at least 0.7 V. When this happens, the capacitor starts to charge because of the positive current in the circuit.

$$v_D = 0.7 \text{ V}$$

$$i_D = i_C = C \cdot \frac{dv_I}{dt}$$

$$v_C(t) = v_I(t) - 0.7 \text{ V}$$

The capacitor charges to the maximum value of:

$$v_{Cmax} = v_{Imax} - 0.7 \text{ V} > 0 \text{ V}$$

From this point on, the input voltage begins to decrease, thus the voltage drop across the diode also decreases below 0.7 V. The diode is now *off*, and the current through the circuit is null:

$$v_D(t) = v_I(t) - v_{Cmax} < 0.7 \text{ V}$$

$$i_D = i_C = 0$$

This point marks the end of the transient regime and the beginning of the permanent regime or steady-state. The voltage on the capacitor remains constant since there is no consumer (load resistance) to discharge the capacitor. The voltage on the capacitor is the output voltage of the circuit.

$$v_O(t) = v_{Cmax} = \text{constant}$$

If the input voltage exhibits a new positive peak, greater than the previous maximum value (v_{Imax}), the diode will once again enter the *on* state, and the capacitor will charge to the value of the new positive peak (v_{Imax} – 0.7 V).

The application of the circuit is *positive peak detector* or *maximum detector* – the circuit identifies and holds the maximum value of the input voltage.

The waveforms for $v_I(t)$, $v_C(t)$ and $v_D(t)$ are depicted in Fig.2.52.

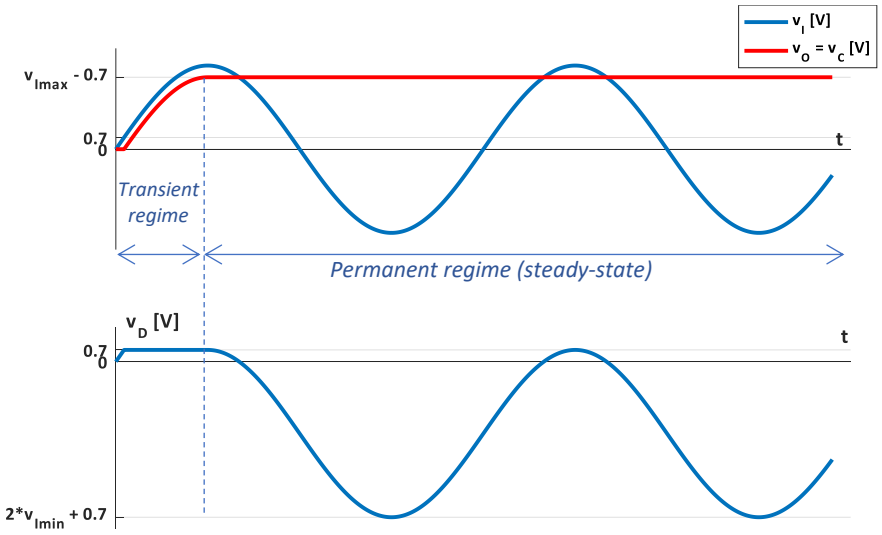


Fig.2.52. Waveforms for the positive peak detector

For the negative peak detector in Fig.2.51. b), the circuit identifies and holds the minimum value of the input voltage. The diode is *on* and the capacitor charges when the input voltage is below -0.7 V.

When the diode is *on*:

$$v_I < -0.7 \text{ V}$$

$$v_O(t) = -v_C(t)$$

$$v_O(t) = v_I(t) + 0.7 \text{ V} < 0 \text{ V}$$

Once the capacitor is charged to the maximum value, the diode is *off*, and the voltage on the capacitor remains constant (capacitor stays charged). This marks the end of the transient regime and the beginning of the steady-state. The waveforms for $v_I(t)$, $v_C(t)$ and $v_O(t)$ are shown in Fig.2.53.

$$v_{Cmax} = - v_{Imin} - 0.7 \text{ V}$$
$$v_{Omin} = v_{Imin} + 0.7 \text{ V} = \text{constant}$$
$$v_D(t) = - v_C(t) - v_I(t) < 0.7 \text{ V}$$
$$v_D(t) = v_O(t) - v_I(t) < 0.7 \text{ V}$$

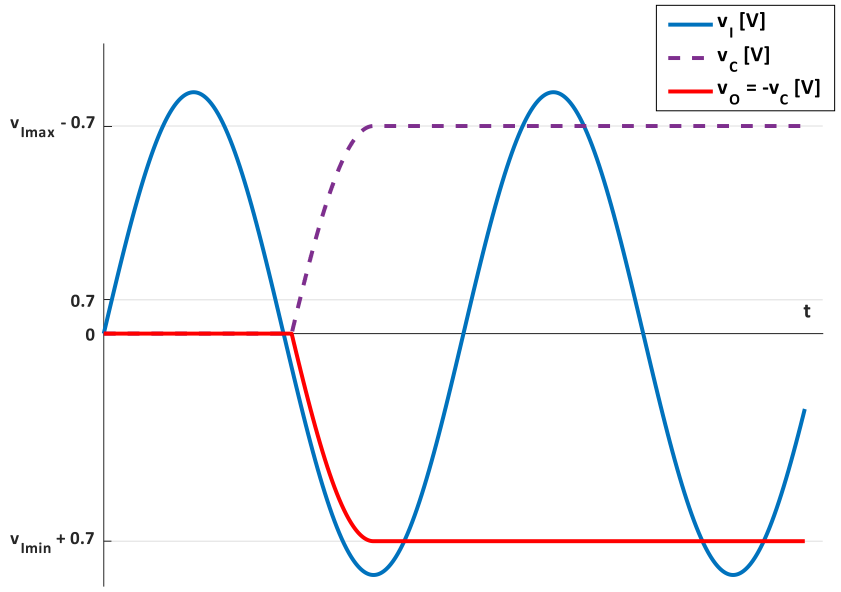


Fig.2.53. Waveforms for the negative peak detector

2.4.2 *DC* switching circuits with the output on *D*

The two *DC* series circuits with the output measured across the diode are shown in Fig.2.54. Notice that the circuits are the same as the ones in Fig.2.51, the difference is that now, the focus is on the diodes, rather than the capacitors.

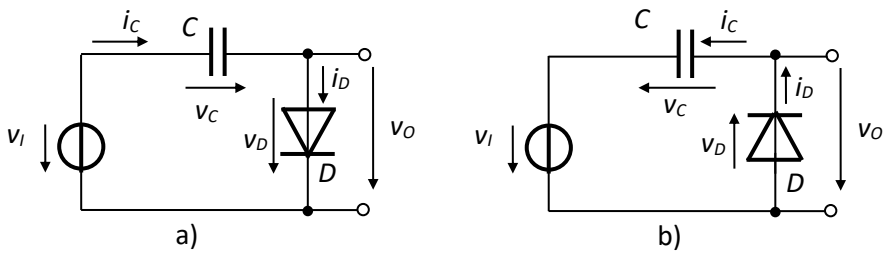


Fig.2.54. *DC* switching circuits with the output on *D*
a) translation towards negative values; b) translation towards positive values.

The output voltage for the circuit in Fig.2.54. a) is the same as the voltage across the diode for the circuit in Fig.2.51. a).

$$v_O(t) = v_D(t) = v_I(t) - v_{Cmax} < 0.7 \text{ V}$$

$$v_O(t) = v_I(t) - v_{Cmax} < 0.7 \text{ V}$$

The output voltage is the same as the input voltage, but with a negative dc offset ($-v_{Cmax}$). This gives the application of the circuit – *translation towards negative values* or *downward translation*. The waveform of the output voltage is $v_D(t)$ in Fig.2.52.

For the circuit in Fig.2.54. b), the output voltage is still measured across the diode, but from cathode to anode:

$$v_O(t) = - v_D(t) > -0.7 \text{ V}$$
$$v_O(t) = v_I(t) + v_{Cmax} > -0.7 \text{ V}$$

The application of the circuit in Fig.2.54. b) is *translation towards positive values* or *upward translation*. The waveforms for $v_I(t)$, $v_C(t)$ and $v_O(t)$ are shown in Fig.2.55.

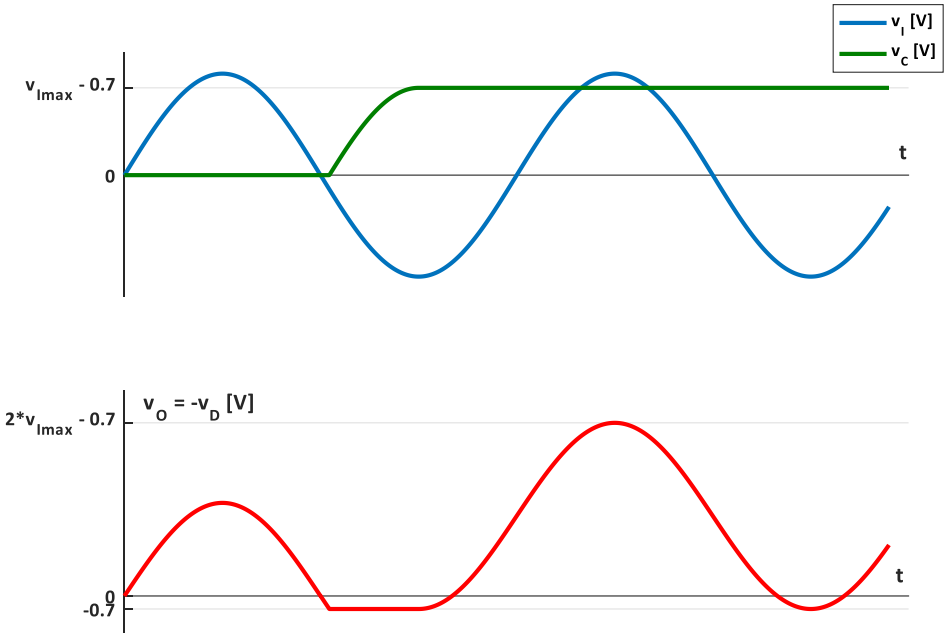


Fig.2.55. Waveforms for $v_I(t)$, $v_C(t)$ and $v_O(t)$ for the upward translation circuit

2.4.3 Applications of *DC* switching circuits

Voltage multipliers

The four series *DC* circuits discussed in the previous section can be connected, so that the output is a dc voltage, with a value twice the amplitude of the input signal. These new circuits are called *voltage doublers*. As a rule, for all voltage multipliers, the output is measured across one or more capacitors.

Two different schematics for the positive voltage doubler are given in Fig.2.56, both consisting of two diodes and two capacitors. The circuit in Fig.2.56. a) shows a positive and a negative peak detector, both with the same input voltage. The output is the difference between the voltages across the two capacitors. For this circuit, there is no common terminal between input and output, hence the input must be obtained from a floating source, such as the secondary of a transformer.

In steady-state, the output voltage v_O is computed as:

$$v_O(t) = v_{O1}(t) - v_{O2}(t)$$
$$v_{O1} = v_{Imax} - 0.7 \text{ V} = \text{constant}$$

$$v_{O2} = v_{Imin} + 0.7\ \text{V} = \text{constant}$$
$$v_O = v_{Imax} - 0.7 - v_{Imin} - 0.7$$
$$v_O = 2 \cdot v_{Imax} - 1.4\ \text{V} = \text{constant}$$

For small values of the amplitude of the input voltage, the circuit will not work as a voltage doubler (e.g., if the input voltage is 1 V, v_{O1} is 0.3 V and v_{O2} is -0.3 V. The output is v_O = 0.6 V, less than the input of 1 V).

The voltage drop across the two diodes in *on* state can be neglected, for large values of the input voltage (e.g., for $\hat{V}_i$ = 100 V, V_O = 198.6 V ≈ 200 V).

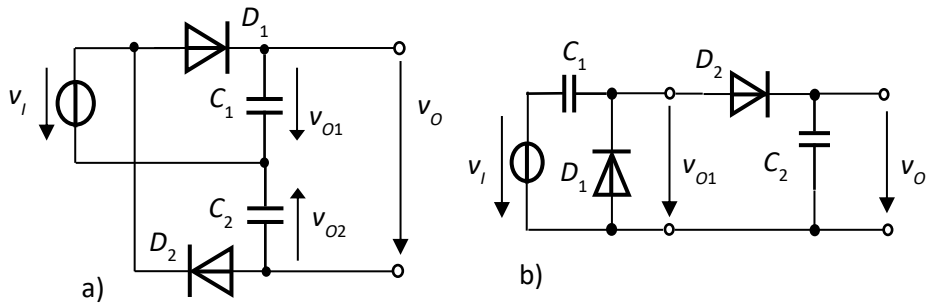


Fig.2.56. Positive voltage doubler
a) positive and negative peak detectors; b) upward translation and positive peak detector.

Another way of obtaining a voltage doubler is shown in Fig.2.56. b), where an upward translation circuit is chained with a positive peak detector. The output of the upward translation circuit is the input for the positive peak detector. In steady-state, v_O is:

$$v_{O1}(t) = v_I(t) + v_{Cmax}$$
$$v_{O1max} = v_{Imax} + v_{Imax} - 0.7\ \text{V}$$
$$v_O = v_{O1max} - 0.7\ \text{V}$$
$$v_O = 2 \cdot v_{Imax} - 1.4\ \text{V} = \text{constant}$$

The output voltage is the same, regardless of which version of the positive voltage doubler is used.

The steady-state waveforms for $v_I(t)$, $v_{C1}(t)$, $v_{O1}(t)$ and $v_O(t)$ for the positive voltage doubler in Fig.2.56. b) are shown in Fig.2.57. By reversing both diodes, a negative voltage doubler is obtained.

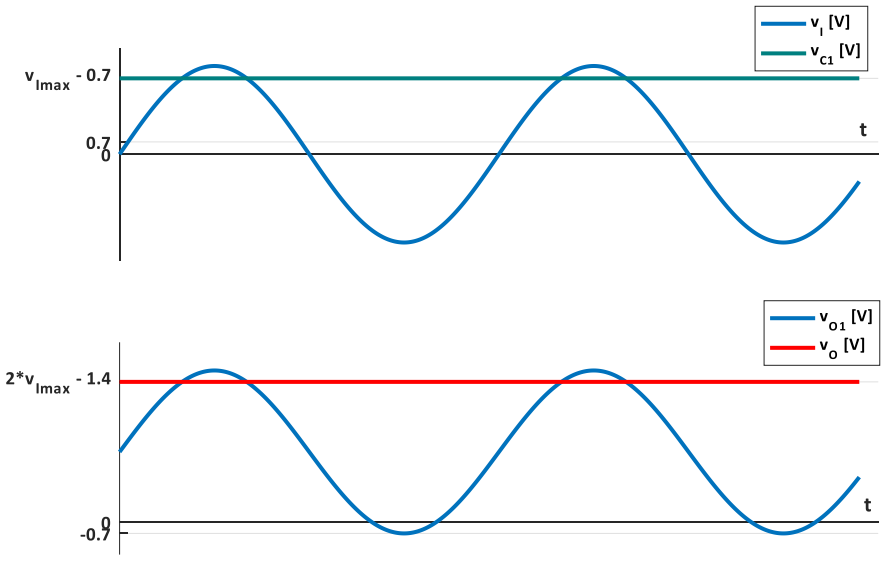


Fig.2.57. Steady-state waveforms for $v_I(t)$, $v_{C1}(t)$, $v_{O1}(t)$ and $v_O(t)$ for the positive voltage doubler in Fig.2.56. b)

Circuits where the dc output voltage is three times the amplitude of the input voltage (ignoring the voltage drop across the conducting diodes) are called *voltage triplers* and are built using three diodes and three capacitors. In general, circuits where the dc output voltage is a multiple of the amplitude of the input voltage are called *voltage multipliers*.

Rectifiers with capacitive filter

Voltage rectifiers are the most used applications of diode circuits, as they represent the first stage in any dc power supply [1]. A dc power supply provides a constant output voltage, with little (millivolts) to (ideally) no variations. The block diagram of a dc power supply is shown in Fig.2.58. The voltage v_r is the output of the rectifier with capacitive filter, while V_O is the output of the dc power supply.

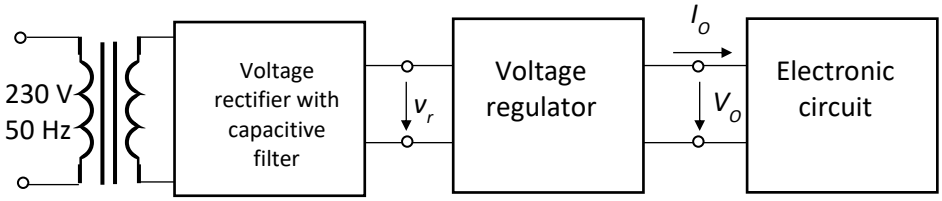


Fig.2.58. Block diagram of a dc power supply

The voltage rectifier with capacitive filter (also known as *DRC* rectifier) is shown in Fig.2.59.

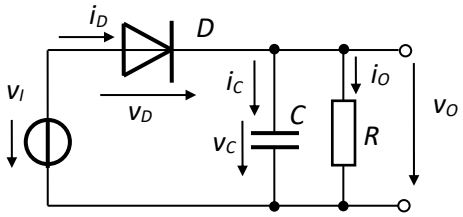


Fig.2.59. *DRC* rectifier

The circuit can be seen either as a half-wave *DR* rectifier with a capacitive load, or as a *DC* positive peak detector with a resistive load. For a half-wave rectifier, the variation or ripple of the output voltage, $\Delta v_O = v_{Imax}$ - 0.7 V. For the positive peak detector, $\Delta v_O = 0$ (Fig.2.60).

The *DRC* rectifier is analysed as a *DC* positive peak detector with resistive load. The capacitor is initially discharged. As long as the diode is *on,* the capacitor charges up to the maximum value:

$$v_{Cmax} = v_{Imax} - 0.7\ \text{V}$$

$$i_D = i_O + i_C = \frac{V_O}{R} + C \cdot \frac{dv_I}{dt}$$

Once the capacitor is charged to the maximum value and v_I decreases, the voltage across the diode drops below 0.7 V, and the diode will be *off*. The capacitor starts to discharge through *R*, until the input voltage is once again large enough to bring the diode back to *on* state. When the diode is *on*, the capacitor charges up to the maximum value and this sequence happens each period. The waveforms of the input and output voltages in steady-state are shown in Fig.2.61.

The output voltage ripple Δv_O depends on the time constant $\tau = R \cdot C$ of the circuit and the period/frequency of the input voltage: the bigger the time constant with respect to the period *T*, the less the capacitor discharges and Δv_O is smaller.

When $\tau >> T$, as in Fig.2.61, the diode is *on* for short amounts of time, t_c, around the maximum values of v_I. Here, the capacitor charges to the maximum value with an amount of electric charge that was previously lost during the discharging time, t_d.

$$T = t_c + t_d$$
$$V_{Omax} = V_{Imax} - 0.7\ V$$

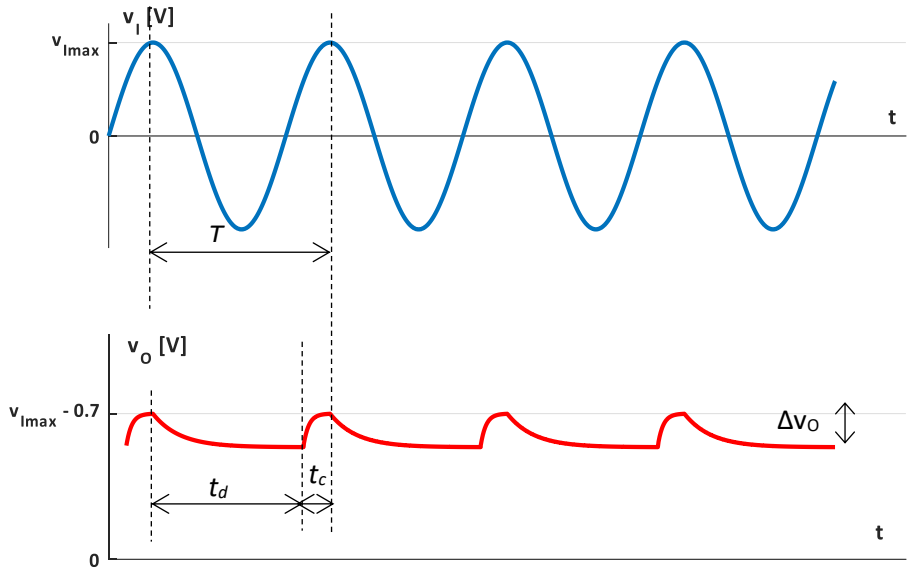


Fig.2.61. *DRC* rectfier waveforms

During the discharge time of the capacitor, t_d, the output voltage decreases as an exponential function of τ, from maximum to minimum. The minimum value is reached at the end of the discharge time, which is assumed to be approximately equal to the period of the signal, for this analysis.

$$t_d \approx T$$
$$V_{Omin} = V_{Omax} - \Delta v_O = V_{Imax} - 0.7 - \Delta v_O$$

The voltage on the capacitor is expressed as:

$$v_c(t) = e^{-\frac{t}{\tau}} \cdot V_C(0) + (1 - e^{-\frac{t}{\tau}}) \cdot V_C(\infty)$$

The purpose of a voltage rectifier with capacitive filter is to obtain an almost dc output voltage, that is a voltage with minimal to no variation. The output voltage varies during the discharge of the capacitor:

$$V_C(0) = V_{Omax}$$
$$V_C(\infty) = 0\ V$$

The voltage on the capacitor after an infinite time is null because the capacitor discharges completely in time unless the voltage starts to increase. With these assumptions, the voltage on the capacitor becomes:

$$v_c(t) = e^{-\frac{t}{\tau}} \cdot V_{Omax}$$
$$V_{Omin} = e^{-\frac{t}{\tau}} \cdot V_{Omax} \approx e^{-\frac{T}{\tau}} \cdot V_{Omax}$$

Since the time constant is significantly larger than the period of the signal, $\tau >> T$, another approximation can be used:

$$e^{-\frac{T}{\tau}} \approx 1 - \frac{T}{\tau}$$

$$V_{Omin} \approx (1 - \frac{T}{\tau})\, V_{Omax}$$

$$V_{Omax} - \Delta v_O \approx V_{Omax} - \frac{T}{\tau} \cdot V_{Omax}$$

$$\Delta v_O \approx \frac{T}{\tau} \cdot V_{Omax}$$

$$\Delta v_O \approx \frac{T}{R \cdot C} \cdot (V_{Imax} - 0.7) = \frac{V_{Imax} - 0.7}{R \cdot C \cdot f}$$

This shows that the bigger the time constant $\tau = R \cdot C$ compared to the period of the input signal T, the smaller the variation of the output voltage Δv_O. Since the load resistor R is not part of the rectifier, but depends on what is connected at the output of the rectifier (R is the input resistance of the circuit connected at the output of the rectifier), small variations of the output voltage are obtained by using larger values of the capacitor.

A capacitor C connected at the output of a diode bridge full-wave rectifier, in parallel with R, transforms the circuit into a full-wave rectifier with capacitive filter. Based on the value of C, the variation of the output voltage decreases from (V_{Imax} – 1.4 V) to a much lower value. The capacitor charges and discharges twice over a period of the input signal, hence the discharge time can be approximated to half a period:

$$t_d \approx \frac{T}{2}$$

The variation (ripple) of the output voltage then becomes:

$$\Delta v_O \approx \frac{T}{2 \cdot R \cdot C} \cdot (V_{Imax} - 1.4)$$

$$\Delta v_O \approx \frac{V_{Imax} - 1.4}{2 \cdot R \cdot C \cdot f}$$

Examples

1. Size a half-wave rectifier with capacitive filter, for which the maximum output voltage ripple Δv_O is 6% of the input voltage. Assume $v_I(t) = 14\sin 2\pi 50t$ [V] [Hz] and $R = 0.2$ kΩ.

Solution:

$$\Delta v_O \approx \frac{6}{100} \cdot 14 = 0.84 \text{ V}$$

$$\Delta v_O \approx \frac{V_{Imax} - 0.7}{R \cdot C \cdot f}$$

$$C \approx \frac{V_{Imax} - 0.7}{R \cdot \Delta v_O \cdot f}$$

$$C \approx \frac{14 - 0.7}{200 \cdot 0.84 \cdot 50} = 1583 \text{ µF}$$

The value obtained for C is the minimum for which the condition is met, any capacitor above 1583 µF can be used (e.g., 2200 µF).

Check that the chosen value meets the condition:

$$\Delta v_O \approx \frac{V_{Imax} - 0.7}{R \cdot C \cdot f}$$

$$\Delta v_O \approx \frac{14 - 0.7}{200 \cdot 2200 \cdot 10^{-6} \cdot 50}$$

$$\Delta v_O \approx 0.6 \text{ V}$$

Check that Δv_O is under 6%:

$$\Delta v_O \approx \frac{0.6}{14} \cdot 100 = 4.28\% < 6\%$$

The design condition is met.

2. What is the maximum value of the output voltage ripple computed at **Problem 1**, in the case of a full-wave rectifier with capacitive filter?

Solution:

For a full-wave rectifier with capacitive filter, two changes must be taken into account: the maximum output voltage is 1.4 V smaller than the maximum input voltage, and the discharge time of the capacitor is approximated to half a period of the input voltage.

$$\Delta v_O \approx \frac{V_{Imax} - 1.4}{2 \cdot R \cdot C \cdot f}$$

$$\Delta v_O \approx \frac{14 - 1.4}{2 \cdot 200 \cdot 2200 \cdot 10^{-6} \cdot 50}$$

$$\Delta v_O \approx 0.28 \text{ V}$$

The percentual value is:

$$\Delta v_O \approx \frac{0.28}{14} \cdot 100 = 2\%$$

Envelope detectors

Information signals are modulated in telecommunications networks, to obtain higher, more efficient transmission rates. By modulation, the properties of the information signal are transferred upon a high-frequency carrier signal.

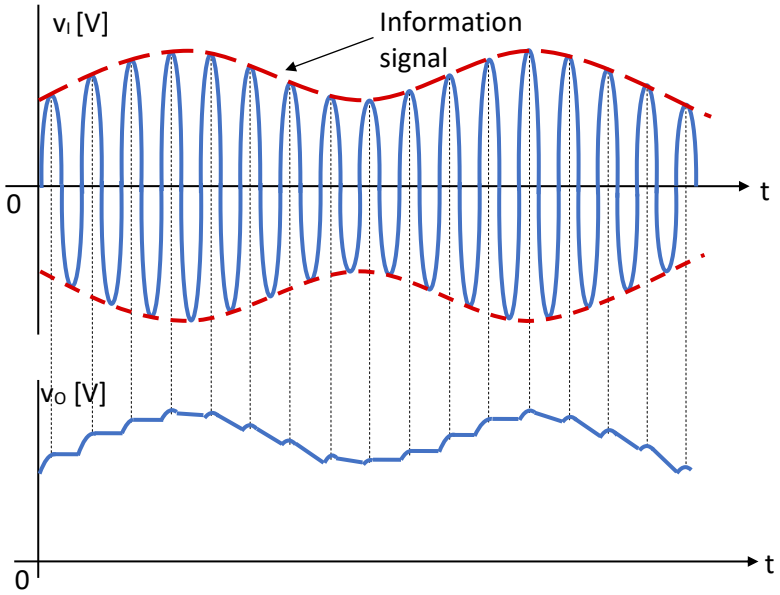


Fig.2.62. Envelope detection of the carrier signal [2]

On the receiver side, demodulation implies extracting the information signal out of the carrier signal. Based on the capacitor's ability to repeatedly charge and discharge in a rectifier with capacitive filter, the output voltage follows the envelope of the modulating (carrier) signal, that is extracting the information signal.

The waveforms for the carrier and demodulated signals are shown in Fig.2.62.

Problems
1. Compute the minimum value of $v_O(t)$ for the circuit in Fig.2.59, for C = 2.2 µF and R = 2 kΩ. Plot $v_I(t)$ and $v_O(t)$ and specify the state of the diode on the plot, for $v_I(t) = 6\sin 2\pi 600t$ [V][Hz]. **2.** Size a half-wave rectifier with capacitive filter, for which the maximum output voltage ripple Δv_O is 8% of the input voltage, when $v_I(t) = 20\sin 2\pi 150t$ [V][Hz] and R = 0.2 kΩ. **3.** Compute the minimum value of $v_O(t)$ for a full-wave rectifier with capacitive filter, for C = 2.2 µF and R = 0.8 kΩ. Draw the circuit and plot $v_I(t)$ and $v_O(t)$ for $v_I(t) = 11\sin 2\pi 60t$ [V][Hz]. **4.** Size a full-wave rectifier with capacitive filter, for which the maximum output voltage ripple Δv_O is 5% of the input voltage, when $v_I(t) = 18\sin 2\pi 300t$ [V][Hz] and R = 0.55 kΩ. Show that the design condition is met.

2.5 Zener diodes

There are diodes for which the breakdown region is not destructive – *Zener diodes,* denoted *ZD*. In forward bias, a Zener diode behaves just like a conventional diode, and a voltage drop of approximately 0.7 V can be measured from anode to cathode. However, this special type of diode exhibits a different behaviour in reverse bias: first, the breakdown voltage V_{Br} is closer to 0 V than it was for conventional diodes; second, when in breakdown, an approximately constant voltage can be measured on it, the Zener voltage, denoted V_Z. Zener diodes are built with standard values of the Zener voltage, ranging from 2 V to 200 V.

2.5.1 The current-voltage characteristic

There are two non-destructive breakdown mechanisms of the *pn* junction in a Zener diode: *the Zener effect* and *avalanche multiplication*.

The Zener effect is present in Zener diodes with 2 V < V_Z < 5 V. The Zener effect is the increase in the number of free carriers, because of the electric field that appears when the *pn* junction is in reverse bias (biased with a negative voltage). The Zener effect appears in semiconductors with high levels of impurities.

Avalanche multiplication occurs in Zener diodes with V_Z > 7 V. When the reverse voltage across the *pn* junction increases, the electric field also increases, which provides the minority carries with enough kinetic energy to break the covalent bonds in the atoms, thus releasing other carriers. These newly released carriers have enough energy to release other carriers, and the process continues, like an avalanche, until there are enough free carriers to ensure the current through the Zener diode.

For Zener diodes with 5 V < V_Z < 7 V, the current can appear as a result of both effects.

There are two ways of representing the current-voltage characteristic $i(v)$ of the Zener diode: either $i_D(v_D)$, where the current and voltage are measured form anode to cathode (like for conventional diodes), or $i_Z(v_Z)$, where the current and voltage are measured from cathode to anode, typical for Zener diodes. The symbol of *ZD* and the two representations for the current-voltage characteristic $i(v)$ are shown in Fig.2.63.

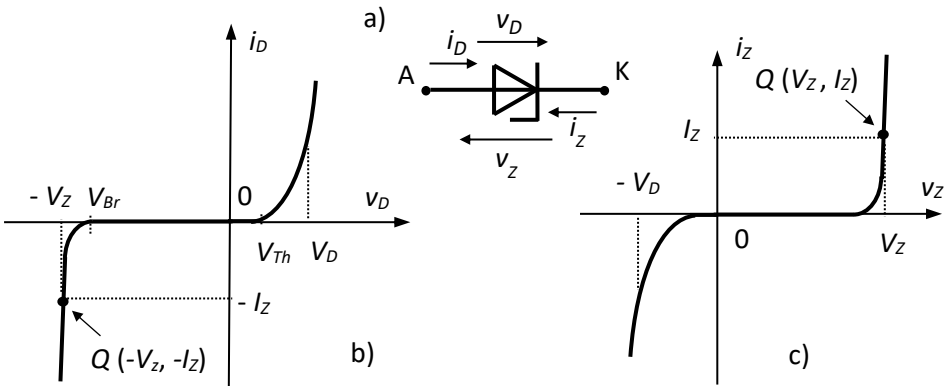


Fig.2.63. Zener diode
a) symbol; b) $i_D(v_D)$; c) $i_Z(v_Z)$.

For the $i_D(v_D)$ characteristic, the 1st quadrant shows the positive i_D and v_D, while i_Z and v_Z are in the 3rd quadrant (negative values). For the $i_Z(v_Z)$ characteristic, the focus is on the reverse bias: i_Z and v_Z are shown as positive in the 1st quadrant, while i_D and v_D (now negative) are found in the 3rd quadrant. Quadrants 1 and 3 are reversed between the two characteristics.

The Zener diode exhibits three states: *on*, *off* and *breakdown* (Fig.2.64). The operating regions, determined by the value of the voltage drop across the diode, are *forward bias* and *reverse bias*. *Breakdown* can be interpreted either as an operating region or as a state. The Zener diode is commonly used in *breakdown*, hence the $i_Z(v_Z)$ characteristic, for which both current and voltage are positive, is preferred.

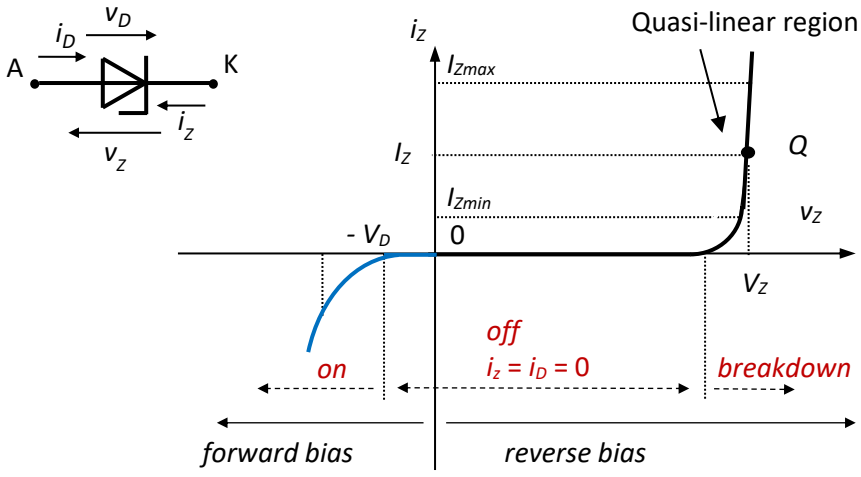


Fig.2.64. Zener diode – operating regions and states

The value of the Zener voltage V_Z is indicated in the name of the Zener diode (i.e., for *ZD*3V3,

V_Z = 3.3 V). In the datasheet, specifications regarding the current are also given. For example, for *ZD*3V3, V_Z = 3.3 V is obtained at a current I_Z = 76 mA. If the current specifications are not met, V_Z will be slightly different from 3.3 V. To ensure a constant V_Z in the quasi-linear around a quiescent point in *breakdown*, the current though *ZD* needs to be within [I_{Zmin}, I_{Zmax}] (Fig.2.64). This ability of the Zener diode to provide a constant voltage drop when the current varies is called *voltage regulation.*

2.5.2 Relative regulation factor

The relative regulation factor, denoted F_Z, measures the regulation capabilities of the Zener diode. The regulation factor is the ratio between the dynamic and the static resistances of *ZD*:

$$F_Z = \frac{r_z}{r_Z}$$

To compute the relative regulation factor, *ZD* must be connected in a circuit, so that it operates in *breakdown* (Fig.2.65). The input voltage must exceed V_Z. Computing the static and dynamic equivalent resistances is done using the same method as for conventional diodes.

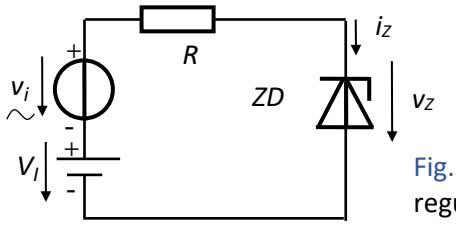


Fig.2.65. Circuit for computing the relative regulation factor of *ZD*

The lower the dynamic resistance, the lower F_Z, meaning better regulation properties (V_Z is more stable, when I_Z varies). For an ideal *ZD,* F_Z = 0.

The behaviour of Zener diodes is also affected by temperature variations. The temperature coefficient *TC* depends on the nominal V_Z and I_Z. For Zener diodes with Zener effect, *TC* < 0, while for Zener diodes with avalanche multiplication, *TC* > 0.

Examples

1. Compute the relative regulation factor for the following *ZDs*, assuming a nominal current I_Z = 5 mA. Which *ZD* exhibits the best regulation properties?

i) *ZD*3V6: V_Z = 3.6 V; r_{zmax} = 88 Ω; r_Z = 0.9 kΩ
ii) *ZD*5V1: V_Z = 5.1 V; r_{zmax} = 50 Ω; r_Z = 1.2 kΩ
iii) *ZD*10: V_Z = 10 V; r_{zmax} = 12 Ω; r_Z = 2 kΩ.

Solution:

$$F_{Zi} = \frac{88}{900} = 0.097$$
$$F_{Zii} = \frac{50}{1200} = 0.041$$
$$F_{Ziii} = \frac{12}{2000} = 0.006$$

*ZD*10 has the best regulation properties (lowest F_Z).

2. Compute the maximum value of I_Z for which *ZD* works as a voltage regulator, knowing that the maximum power dissipation for *ZD*10 is P_{dmax} = 0.3 W.

Solution:

$$I_{Zmax} = \frac{P_{dmax}}{V_Z}$$

$$I_{Zmax} = \frac{0.3}{10} = 0.03 \text{ A} = 30 \text{ mA}$$

2.5.3 Applications of the Zener diode

Any circuit with Zener diodes and resistors can be used as a voltage limiter (clamp). Moreover, since V_Z is approximately constant when I_Z varies within specified boundaries, *ZD* can be used in voltage regulator circuits.

Double voltage limiter

Double voltage limiters are obtained by replacing the conventional diodes in the circuits in Fig.2.18 c) and d) with Zener diodes, as shown in Fig.2.66. a) and b).

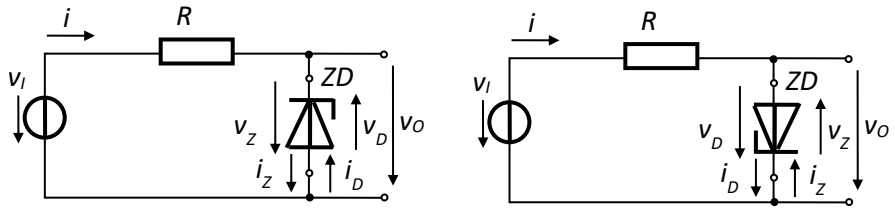


Fig.2.66. Asymmetric double voltage limiters with *ZD*

The equations that describe the circuit in Fig.2.66. a) are:

$$v_I = i_Z \cdot R + v_O$$

$$v_O = v_Z$$

$$v_I = -i_D \cdot R + v_O$$

$$v_O = -v_D$$

The three equivalent circuits, based on the states of *ZD,* are shown in Fig.2.67.

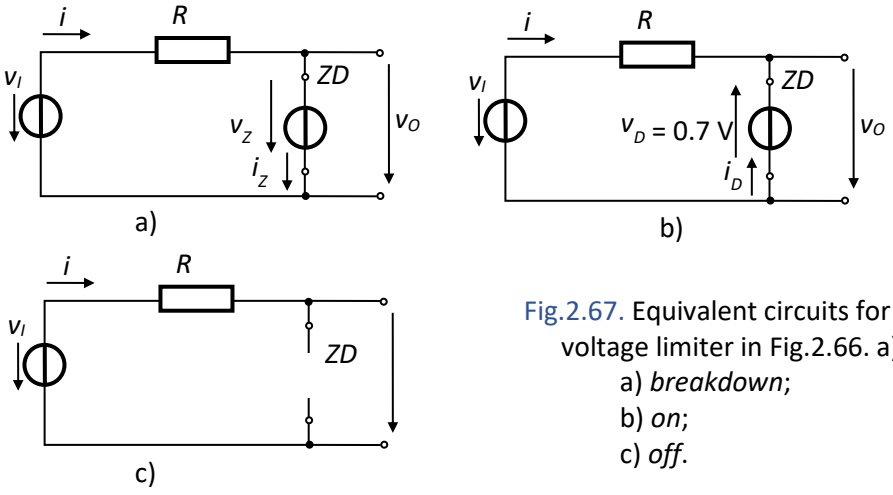


Fig.2.67. Equivalent circuits for the voltage limiter in Fig.2.66. a)
a) *breakdown*;
b) *on*;
c) *off*.

ZD is in *breakdown* for $v_I > V_Z$, and the output voltage is limited to $V_{Omax} = V_Z$. *ZD* is *on* for $v_I < -0.7$ V, and the output voltage is limited to $V_{Omin} = -V_D = -0.7$ V. Finally, *ZD* is *off* for $-0.7\text{ V} < v_I < V_Z$, and $v_O = v_I$. The VTC $v_O(v_I)$ and the waveforms for v_I and v_O are depicted in Fig.2.68.

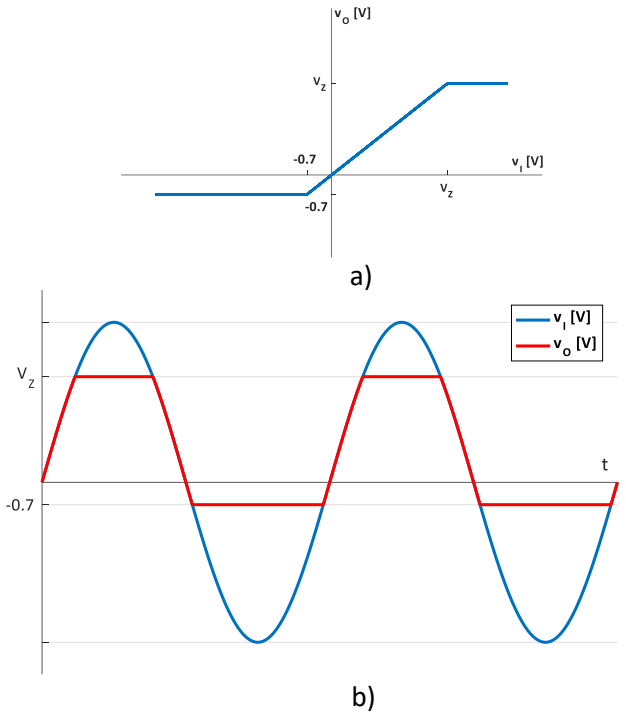


Fig.2.68. Asymmetric double voltage limiter a) VTC $v_O(v_I)$; b) waveforms.

A symmetrical double voltage limiter is obtained by using two identical *ZD*s ($V_{Z1} = V_{Z2}$), connected in antiparallel, at the output of the circuit (Fig.2.69. a). The VTC of the symmetrical double voltage limiter is shown in Fig.2.69. b).

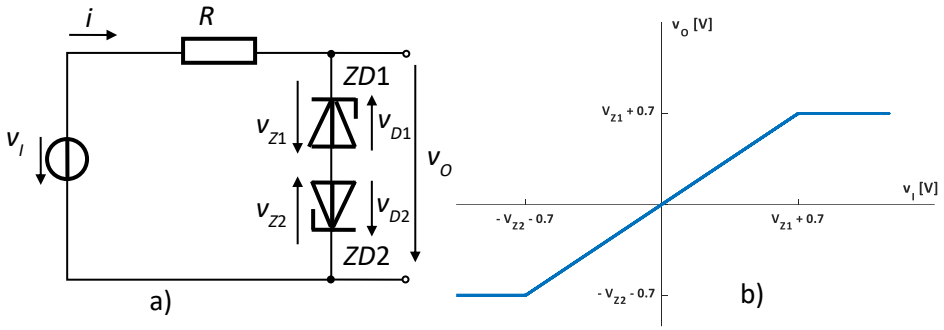


Fig.2.69. Symmetrical voltage limiter
a) circuit; b) VTC $v_O(v_I)$.

For $v_I > (V_{Z1} + 0.7\text{ V})$, *ZD*1 is in *breakdown, ZD*2 is *on*, and $V_{Omax} = V_{Z1} + 0.7$ V.
For $v_I < -(V_{Z2} + 0.7\text{ V})$, *ZD*1 is *on*, *ZD*2 is in *breakdown,* and $V_{Omin} = -V_{Z2} + 0.7$ V.
For $-(V_{Z2} + 0.7\text{ V}) < v_I < (V_{Z1} + 0.7\text{ V})$, ZD*1* and ZD*2* are *off*, and $v_O = v_I$. In this case, there is no current through the circuit, so the voltage drop across *R* is null.

Example

Design a double voltage limiter with V_{Omax} = 7.5 V and V_{Omin} = -4 V, when the input voltage is $v_I(t) = 12\sin\omega t$ [V].
a) deduce and plot the VTC $v_O(v_I)$
b) plot $v_I(t)$ and $v_O(t)$
c) compute R so that the maximum power dissipation across ZD is 0.4 W.

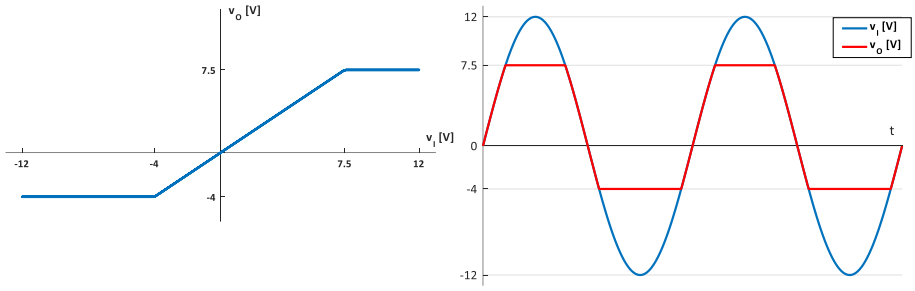
Solution:

a) The circuit is the one in Fig.2.69, where $ZD1$ is $ZD6V8$ and $ZD2$ is $ZD3V3$.

$$v_I > (6.8\text{ V} + 0.7\text{ V});\ V_{Omax} = 7.5\text{ V}$$
$$v_I < -(3.3\text{ V} + 0.7\text{ V});\ V_{Omin} = -4\text{ V}$$
$$-4\text{ V} < v_I < 7.5\text{ V};\ v_O = v_I$$

The VTC $v_O(v_I)$ is shown in Fig.2.70. a).

b) The waveforms are depicted in Fig.2.70. b).



a) b)

Fig.2.70. Asymmetric double voltage limiter with V_{Omax} = 7.5 V and V_{Omin} = -4 V
a) VTC $v_O(v_I)$; b) waveforms.

c) The voltage drop across R is computed as:

$$v_R = i \cdot R = v_I - v_O$$

The elements of the circuit are connected in series, so the same current goes through each of them. This current can go clockwise or counterclockwise. When $v_O = v_I$, the current is null, since both ZDs are *off*. The extreme values of the current are obtained when the output voltage is at the peak (limit) values. Both cases are analysed, to determine the maximum value of the current, which results in the maximum power dissipation.

i) $v_I > 7.5$ V for $ZD1$ in *breakdown*

$$V_{Imax} = 12\text{ V}$$
$$V_{Omax} = 7.5\text{ V}$$
$$i \cdot R = 4.5\text{ V}$$
$$I_{Z1max} = \frac{P_{dmax}}{V_{Z1}}$$
$$I_{Z1max} = \frac{0.4}{6.8}$$
$$I_{Z1max} \approx 59\text{ mA}$$
$$I_{Z1max} = i$$

$$R = \frac{4.5}{59 \cdot 10^{-3}} = 76\ \Omega$$

ii) $v_I < -4$ V for *ZD*2 in *breakdown*

$$V_{Imin} = -12\ \text{V}$$
$$V_{Omin} = -4\ \text{V}$$
$$i \cdot R = -8\ \text{V}$$
$$I_{Z2max} = \frac{P_{dmax}}{V_{Z2}}$$
$$I_{Z2max} = \frac{0.4}{3.3}$$

$$I_{Z2max} \approx 121\ \text{mA}$$
$$I_{Z2max} = -\ i$$

$$R = \frac{-8}{-121 \cdot 10^{-3}} = 66\ \Omega$$

The final value of *R* is the greatest of the two, thus $R = 76\ \Omega$.
In this case, for $v_I > 7.5$ V, the maximum value of the current is 59 mA, while for $v_I < -4$ V, the maximum current through *ZD*2 is 105 mA (8 V/76 Ω), below the maximum accepted value of 121 mA.

If *R* is chosen as the smallest value, $R = 66\ \Omega$, the maximum current through *ZD*1 is 68 mA. The power dissipation across *ZD*1 becomes:

$$P_{dZ1max} = I_{Z1max} \cdot V_{Z1}$$
$$P_{dZ1max} = 68 \cdot 6.8 = 0.46\ \text{W} > 0.4\ \text{W}$$

In this case, *ZD*1 might be destroyed.

Parametric voltage regulator

The block diagram of the dc power supply in Fig.2.58 contains a dc voltage regulator, right after the rectifier with capacitive filter. A voltage regulator maintains a constant output voltage (ideally), when the input voltage, load current, temperature, etc. vary within specified limits.

The parametric voltage regulator with *ZD* is shown in Fig.2.71. The Zener diode must be in *breakdown*, so that the output voltage is regulated (stable, constant). The current through the Zener diode must also be constant, or with as little variation as possible.

$$V_O = V_Z$$
$$i_R = i_Z + I_O$$
$$i_Z = i_R - I_O$$
$$i_R = \frac{v_I - V_Z}{R}$$
$$I_O = \frac{V_O}{R_L} = \frac{V_Z}{R_L}$$
$$i_Z = \frac{v_I - V_Z}{R} - \frac{V_Z}{R_L}$$

The current through the Zener diode depends on the input voltage, resistor *R* and the load resistance. The value of *R* must be chosen so that the current through the Zener diode is

$i_Z \in [I_{Zmin}; I_{Zmax}]$. Assuming the input voltage is $v_I \in [V_{Imin}; V_{Imax}]$ and the output current is $I_O \in [I_{Omin}; I_{Omax}]$, the extreme values of the current through the Zener diode are computed as:

$$I_{Zmin} = \frac{V_{Imin} - V_Z}{R_{max}} - \frac{V_Z}{R_{Lmin}} = \frac{V_{Imin} - V_Z}{R_{max}} - I_{Omax}$$

$$I_{Zmax} = \frac{V_{Imax} - V_Z}{R_{min}} - \frac{V_Z}{R_{Lmax}} = \frac{V_{Imax} - V_Z}{R_{min}} - I_{Omin}$$

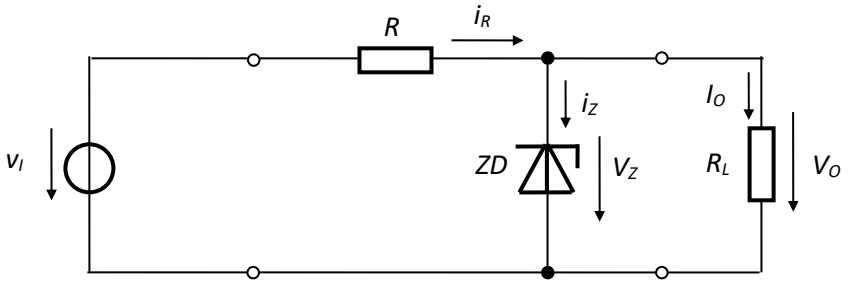


Fig.2.71. Parametric voltage regulator with *ZD*

Consequently, the range of values for R is $R \in [R_{min}; R_{max}]$. If, by any chance, the computed values result in $R_{max} < R_{min}$, the circuit cannot work as a voltage regulator.

$$R_{max} = \frac{V_{Imin} - V_Z}{I_{Zmin} + I_{Omax}}$$

$$R_{min} = \frac{V_{Imax} - V_Z}{I_{Zmax} + I_{Omin}}$$

The absolute voltage regulation factor, F_{Va}, is the ratio between the variations of the output and input voltages. This factor does not include the nominal values, only the absolute variations. Ideally, $F_{Va} = 0$.

$$F_{Va} = \frac{\Delta v_O}{\Delta v_I}$$

The relative voltage regulation factor, F_V, which includes both the variations and the nominal values of the output and input voltages, is defined as:

$$F_V = \frac{\Delta v_O / V_O}{\Delta v_I / V_I}$$

$$F_V = \frac{\Delta v_O}{\Delta v_I} \cdot \frac{V_I}{V_O}$$

To compute the relative regulation factor, the Zener diode is modelled using its static resistance, in the dc equivalent schematic (Fig.2.72), and using its dynamic resistance, in the ac (small-signal) schematic.

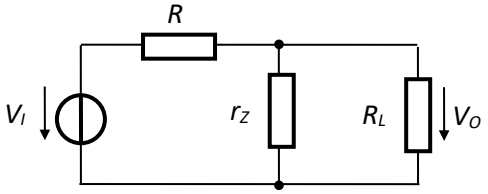


Fig.2.72. Parametric voltage regulator with *ZD*: dc equivalent schematic

$$V_O = \frac{R_L || r_Z}{R_L || r_Z + R} \cdot V_I; \qquad \Delta V_O = \frac{R_L || r_z}{R_L || r_z + R} \cdot \Delta V_I$$

$$\frac{V_I}{V_O} = \frac{R_L || r_Z + R}{R_L || r_Z}; \qquad \frac{\Delta V_O}{\Delta V_I} = \frac{R_L || r_z}{R_L || r_z + R}$$

$$F_V = \frac{R_L || r_z}{R_L || r_z + R} \cdot \frac{R_L || r_Z + R}{R_L || r_Z}$$

In practical implementations, both the static and the dynamic resistance are much smaller than R_L. The relative regulation factor is then approximated to:

$$F_V = \frac{r_z}{r_z + R} \cdot \frac{r_Z + R}{r_Z}$$

$$F_V = \frac{r_z}{r_Z} \cdot \frac{r_Z + R}{r_z + R} \approx \frac{r_z}{r_Z} = F_Z$$

The lower the relative regulation factor, the better the voltage regulator. If R is significantly bigger than r_z and r_z, the second ratio can further be approximated to 1. In this case, the relative regulation factor F_V becomes equal to the regulation factor of the Zener diode, F_Z.

Example

Find R for a parametric voltage regulator with ZD, with V_O = 9.1 V; $v_I \in$ [12; 16] V; $I_O \in$ (10; 40) mA and the dynamic resistance of ZD is r_z = 5 Ω. Compute Δv_O for the final circuit.

Solution:

Since V_O = 9.1V, the Zener diode ZD9V1, 1 W is selected. For this ZD, V_Z = 9.1 V at I_Z = 28 mA and I_{Zmin} = 8 mA, I_{zmax} = 100mA.

$$R_{max} = \frac{12 - 9.1}{8 + 40} = 60.4\ \Omega$$

$$R_{min} = \frac{16 - 9.1}{100 + 10} = 62.7\ \Omega$$

The standard value of R = 62 Ω is selected.

To determine Δv_O, the relative regulation factor is computed, knowing that r_z = 5 Ω (given) and r_Z = 325 Ω (9.1 V/28 mA).

$$F_V = \frac{5}{325} \cdot \frac{325 + 62}{5 + 62}$$

$$F_V \approx 0.088 = \frac{\Delta v_O}{\Delta v_I} \cdot \frac{V_I}{V_O}$$

The equation is solved for Δv_O:

$\Delta v_I = V_{Imax} - V_{Imin}$ = 4 V; V_O = 9.1 V; $V_I = (V_{Imax} + V_{Imin})/2$ = 14 V.

$$\Delta v_O = 0.088 \cdot 4 \cdot \frac{9{,}1}{14}$$

$$\Delta v_O \approx 0.23\ \text{V}$$

For V_O = 9.1 V, a variation of 4 V in the input voltage determines a variation of 0.23 V in the output voltage.

Voltage reference

In complex voltage regulators, the Zener diode can be used as a voltage reference, due to its ability of maintaining a constant voltage drop, when operating in the *breakdown region*.

For voltage references, the current I_Z must also be maintained constant: either by using a current source, or by using a resistor in series with *ZD* (Fig.2.73).

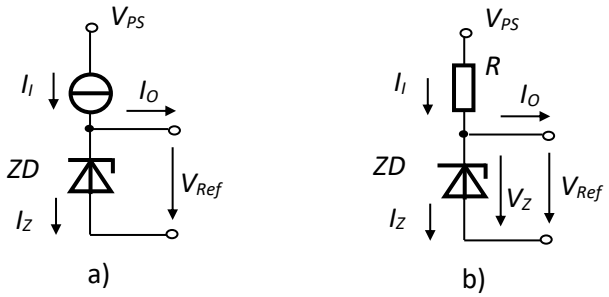


Fig.2.73. Voltage reference with *ZD*
a) biasing using a dc current source; b) biasing using a resistor.

The value of *R* in Fig.2.7. b) is sized so that *ZD* operates at the nominal current I_Z:

$$R = \frac{V_{PS} - V_{Ref}}{I_I} = \frac{V_{PS} - V_Z}{I_I}$$

$$I_I = I_Z + I_O$$

In practical circuits, the current I_O drawn from the reference source must by significantly lower than the current the Zener diode, so that:

$$I_I \approx I_Z$$

Problems

1. Design and size an asymmetric double voltage limiter using *ZD*12, with I_Z = 21 mA.
a) Draw the circuit. Deduce and plot the VTC $v_O(v_I)$ for $v_I(t) = 14\sin\omega t$ [V].
b) Plot $v_I(t)$ and $v_O(t)$ for $v_I(t) = 14\sin\omega t$ [V].

2. Design and size a symmetric voltage limiter, to ± 8.9 V.
a) Draw the circuit. Select an appropriate Zener diode and specify the values of V_Z and I_Z.
b) Deduce and plot the VTC $v_O(v_I)$ for $v_I(t) = 10\sin\omega t$ [V].
c) Plot $v_I(t)$ and $v_O(t)$ for $v_I(t) = 10\sin\omega t$ [V].
d) Compute *R,* so that the maximum power dissipation on *ZD* is 1 W.

3. Compute the relative regulation factor F_V for a parametric voltage regulator with *ZD*, for which $v_I \in [8.5; 14]$ V; $V_O \in (6.18; 6.22)$ V.

4. Determine the value of resistor *R* for a parametric voltage regulator with *ZD*, for which V_O = 12 V; $v_I \in [15; 20]$ V; $I_O \in (10; 40)$ mA the dynamic resistance of *ZD* is r_z = 9 Ω. Compute Δv_O for the final circuit.

5. Design and size a voltage reference using a *ZD* and a resistor, with V_{ref} = 11 V at I_Z = 23 mA. The dc power supply is considered big enough to ensure the proper functioning of the circuit.

2.6 LEDs and photodiodes

The *pn* junction of a *light-emitting diode* (*LED*) converts electrical energy into light. The bigger the current through the LED, the more photons are emitted, hence the brighter the light. The arrows pointing outward on the LED's symbol represent the emission of photons (light) (Fig.2.74). To emit light, the LED must be in *forward bias*, and the voltage drop across it needs to exceed the threshold voltage of the LED. Different colours of the emitted light are obtained by doping the *pn* junction with alloys of Ga, As, In.

The threshold voltage above which the light becomes visible, as well as its colour, depends on the material the LED is made of (Fig.2.74). The threshold voltage is commonly within [1.2; 2.5] V. The breakdown voltage for LEDs is closer to 0 than for conventional diodes, meaning LEDs get destroyed a lot easier.

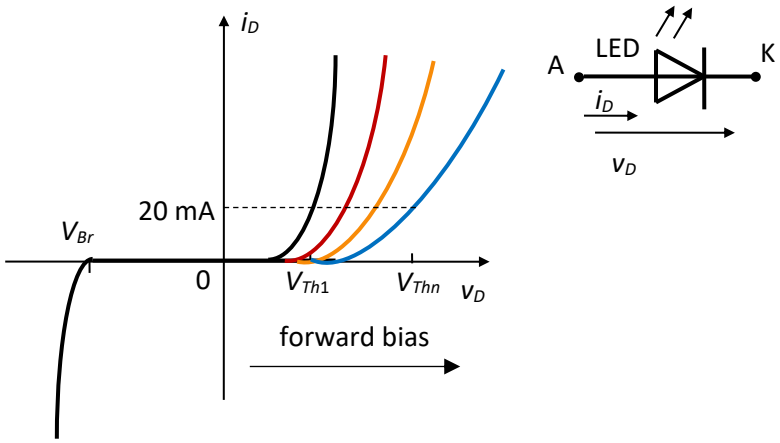


Fig.2.74. LED
a) $i_D(v_D)$ for different colours of LEDs; b) symbol.

Typical values for the current through an LED are within [5; 20] mA. To control the current through the LED, a resistor *R* is placed in series (Fig.2.75); its value is determined based on the desired current through the LED.

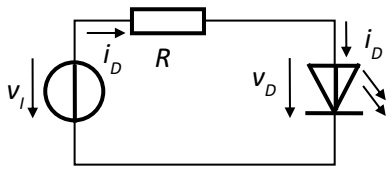


Fig.2.75. Simple circuit with LED and *R*

$$i_D \cdot R = v_I - v_D$$

$$R = \frac{v_I - v_D}{i_D}$$

LEDs are used in optical voltage level indicators, traffic lights, display panels, measuring instruments, etc. LEDs can be connected in series or in parallel (Fig.2.76), each type of connection with its own advantages and drawbacks.

For three LEDs connected in series (Fig.2.76. a), the conditions are:

$$v_I > 3 \cdot v_D \qquad i = i_D \qquad v_O = 3 \cdot v_D$$

For three LEDs connected in parallel (Fig.2.76. b)), the conditions are:

$$v_I > v_D \qquad i = 3 \cdot i_D \qquad v_O = v_D$$

When the LEDs are connected in series, the required input voltage is bigger, but the circuit needs less current than the parallel connection.

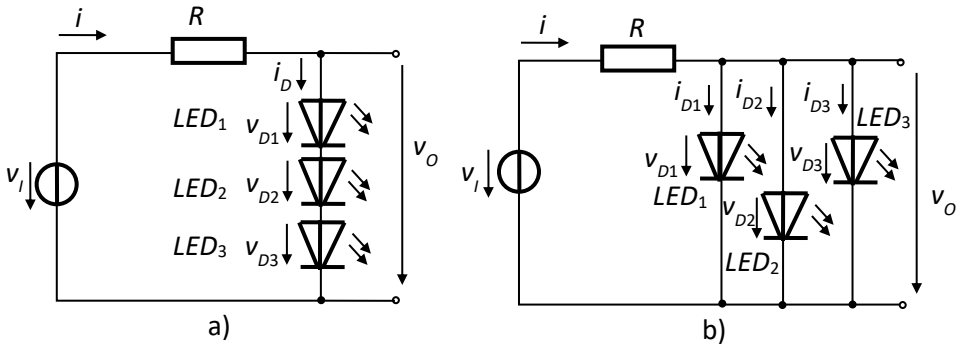


Fig.2.76. Simple circuits with LEDs
a) in series; b) in parallel.

A *photodiode* is a *pn* junction sensitive to light (photosensitive), meaning it converts light into an electrical signal. The arrows pointing inward on the photodiode's symbol (Fig.2.77) represent the absorbed luminous radiation. To generate current, the photodiode is used in reverse bias/breakdown, like a Zener diode. The current-voltage characteristic of a photodiode is shown in Fig.2.77. When there is no light, the current is almost null. When the light increase, the reverse current also increases. Photodiodes can be found in smoke and fire detectors, medical instruments, solar panels, etc.

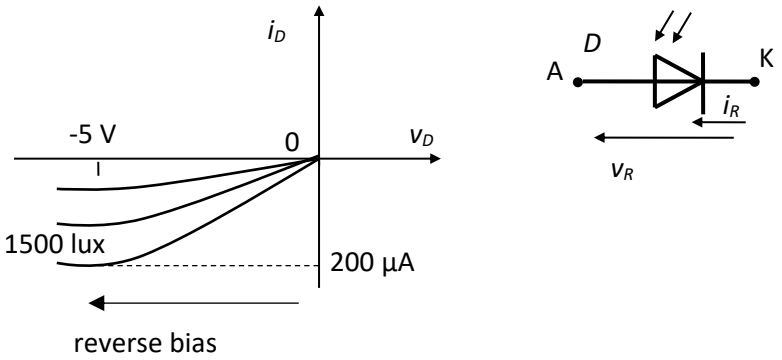


Fig.2.77. Photodiode
a) $i_D(v_D)$ for various photodiodes; b) symbol.

Example

Compute R for the circuit in Fig.2.75, if V_I = 5 V, and the current through the LED is 10 mA.

Solution:

Assume V_D = 2 V when the LED is *on*:

$$R = \frac{5 - 2}{10 \cdot 10^{-3}} = 300\ \Omega$$

Problems
1. Compute *R* for a circuit with four LEDs connected in series, if V_I = 10 V, and the maximum current through the LEDs is 20 mA. What is V_{Imin} for which the LEDs are *on*? **2.** Compute *R* for a circuit with four LEDs connected in parallel, if V_I = 10 V, and the maximum current through the LEDs is 20 mA. What is V_{Imin} for which the LEDs are *on*?

Chapter 3

ELECTRONIC AMPLIFIERS

In this chapter, you will learn:

- what electronic amplifiers are
- types of amplifiers
- how electronic amplifiers are supplied
- parameters of electronic amplifiers
- how electronic amplifiers are modelled
- voltage transfer characteristics of electronic amplifiers.

****

3.1 Introduction

Electronic amplifiers are fundamental circuits, found in almost any signal processing system [1]. This chapter treats the amplifier as a functional block, analysing its external characteristics, without going into details regarding the internal structure.

Whenever the amplitude of a processed signal is small (10^{-3} or less), the signal can easily be "drowned" in noise, so an increase in amplitude becomes mandatory. This is achieved by the electronic amplifier.

An electronic amplifier is a three-port circuit, with two inputs and one output. Signals are applied at the inputs, and the amplified (magnified) signal is collected from the output.

The signals applied at the inputs are the *input signal* and the *power supply*, as presented in Fig.3.1, where the electronic amplifier is depicted as a "black-box".

For electronic amplifiers, the input is a variable signal (ac), while the power supply is a dc signal. The variable component of the input is found at the output, with the same type of variation, same frequency/period, but with greater power. Since the power at the output is greater than the power at the input, the electronic amplifier is an active circuit. The additional power at the output comes from the power supply, without which the electronic amplifier cannot function.

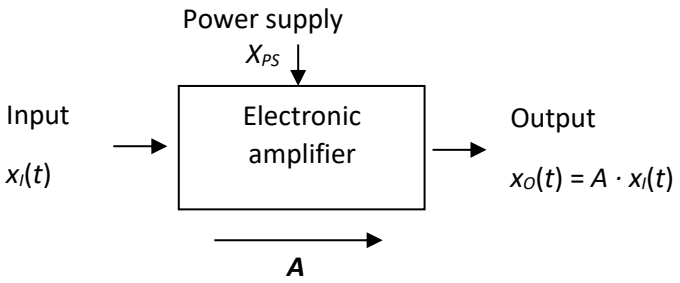


Fig.3.1. "Black-box" representation of the electronic amplifier

The parameter that defines the electronic amplifier is the *gain* (*amplification*), denoted *A* in Fig.3.1. This value shows the ration between output and input, in other words, how many times the output is bigger than the input. The gain *A* is a constant value, that does not depend on the amplitude of the input signal.

$$x_O(t) = A \cdot x_I(t)$$

$$A = \frac{x_O(t)}{x_I(t)}$$

The input and output are directly proportional, hence electronic amplifiers are active and linear circuits, in the active region.

3.2 Types of electronic amplifiers

Based on the nature of input and output signals (voltages or currents), denoted $x_I(t)$ and $x_O(t)$ in Fig.3.1, there are four types of electronic amplifiers:

- voltage amplifier, $x_I(t)$ and $x_O(t)$ are voltages - $v_I(t)$ and $v_O(t)$
- current amplifier, $x_I(t)$ and $x_O(t)$ are currents - $i_I(t)$ and $i_O(t)$
- transconductance amplifier, $x_I(t)$ is voltage - $v_I(t)$, and $x_O(t)$ is current - $i_O(t)$
- trans-resistance amplifier, $x_I(t)$ is current - $i_I(t)$, and $x_O(t)$ is voltage - $v_O(t)$.

For a voltage amplifier, the absolute value of the voltage gain A_V is computed as the ratio between the amplitude of the output voltage and the amplitude of the input voltage. The voltage gain is dimensionless.

$$|A_V| = \frac{\widehat{V_O}}{\widehat{V_I}}$$

For a transconductance amplifier, the absolute value of the transconductance gain $A_{I/V}$ is computed as the ratio between the amplitude of the output current and the amplitude of the input voltage. Other notations for the transconductance gain are G_m or g_m. The transconductance gain is measured in Siemens.

$$|A_{I/V}| = \frac{\widehat{I_O}}{\widehat{V_I}} \text{ [S]}$$

Another way of classifying electronic amplifiers is by analysing the input-output relation. If the output increases with the increase of the input, the amplifier is *noninverting,* and the gain A_V is positive. For a noninverting amplifier, the input and output signals are in phase (Fig.3.2. a).

If the output decreases with the increase of the input, the amplifier is *inverting,* and the gain *A* is negative. For an inverting amplifier, the input and output signals are in anti-phase (opposite phase) (Fig.3.2. b); the output is shifted with 180° (half a period) with respect to the input. Even if the gain is negative, the amplitude of the output signal is still greater than the amplitude of the input signal.

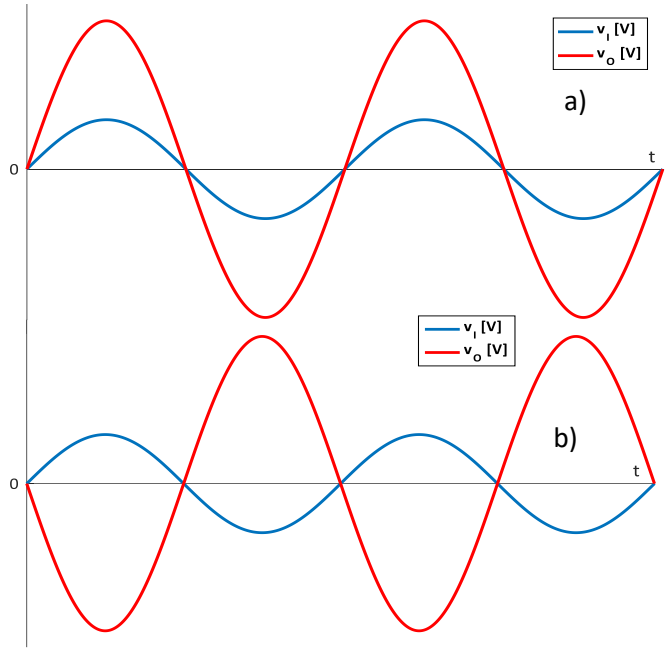


Fig.3.2. Voltage amplifier - waveforms
a) noninverting; b) inverting.

When the gain is $-1 < A < 1$, the amplitude of the output signal is smaller than the amplitude of the input signal, and the circuits are called *attenuators*.

Finally, electronic amplifiers can be classified based on the electronic device that performs the amplification – operational amplifier, transistor, etc. Electronic amplifiers are analysed from the point of view of the active electronic device, relationship between input and output, types of input and output signals.

3.3 Supplying electronic amplifiers

In most cases, electronic amplifiers are supplied using dc voltage sources, but dc current sources can also be used.

When a single source is used, the supply is called *single supply* or *unipolar supply*, and the dc sources can be positive or negative (Fig.3.3 a) and b). The remaining supply terminal is grounded. When the amplifier is supplied using two sources, the term is *differential supply*. One of the sources is positive, while the other one is negative, and their absolute values are usually equal, as shown in Fig.3.3. c).

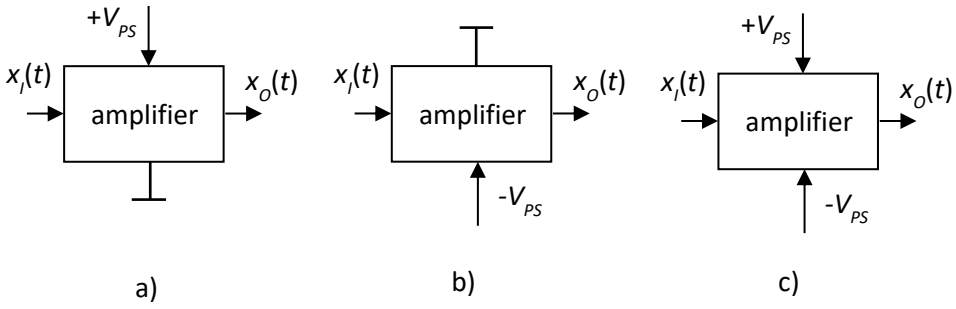


Fig.3.3. Amplifier supply
a) unipolar, positive; b) unipolar, negative; c) differential.

The output power of a differential supply amplifier is greater than the output power of a single supply amplifier, which explains why the differential supply is preferred. Supply voltage specifications (i.e., extreme values of the supply voltage, unipolar, differential or both types of supply) are given in the datasheet of any electronic device or integrated circuit that can be used as amplifier.

3.4 Amplifier parameters

The behaviour of an electronic amplifier, connected in a circuit, depends on a series of parameters, out of which the most important ones are:

- gain
- input resistance
- output resistance
- active region
- gain-bandwidth product (*GBW*).

The gain *A*

The gain *A* shows how many times the output signal is bigger than the input signal. Three types of gain can be determined: voltage gain A_V, current gain A_I and power gain A_P, all of them being dimensionless.

$$A_V = \frac{V_O}{V_I}$$

$$A_I = \frac{I_O}{I_I}$$

$$A_P = \frac{P_O}{P_I} = \frac{V_O \cdot I_O}{V_I \cdot I_I}$$

$$A_P = A_V \cdot A_I$$

The input resistance R_i

The input resistance is the resistance “seen” by the input source, from the point it is applied to, towards ground (0 V). The meaning of this resistance is that the amplifier draws or absorbs current from the input source.

The input resistance is computed using Ohm's law, as the ratio between the input voltage and the current drawn from the input source (Fig.3.4):

$$R_i = \frac{v_i}{i_i}$$

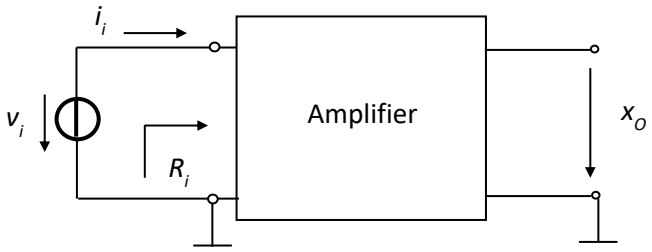


Fig.3.4. Circuit for computing R_i

The output resistance R_o

The output resistance determines changes of the output voltage when the amplifier delivers a current through the load. R_o can be seen as the resistance from output towards input when the input is grounded. The circuit for computing R_o is shown in Fig.3.5. A test voltage source is applied at the output of the circuit, and the output resistance is the ratio between the test voltage and the current draw by the output of the circuit:

$$R_o = \frac{v_{test}}{i_{test}}$$

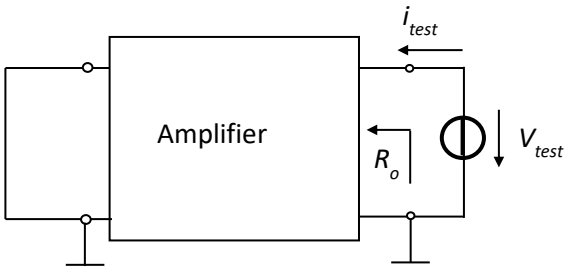


Fig.3.5. Circuit for computing R_o

The active region

An electronic amplifier behaves as an amplifier only in the active region. Here, the VTC $x_O(x_I)$ is linear, and its slope is the gain of the amplifier. The range of values of the input signal for which the amplifier works in the active region depends on the value of the power supply and the gain of the amplifier.

When the input signal is outside the active region of the amplifier, the output is limited to the values of the supplies ($+V_{PS}$ and/or $-V_{PS}$). In this case, the shape of the output signal is no longer identical to the shape of the input signal (the output signal is limited/clamped), thus the gain can no longer be computed as the ratio between the amplitudes of the output and input signals.

The gain-bandwidth product *GBW*

The behaviour of any electronic circuit is specified for a certain frequency range of the input signal.

Electronic amplifiers exhibit a bandpass filter behaviour, for which the amplifier-frequency characteristic is shown in Fig.3.6.

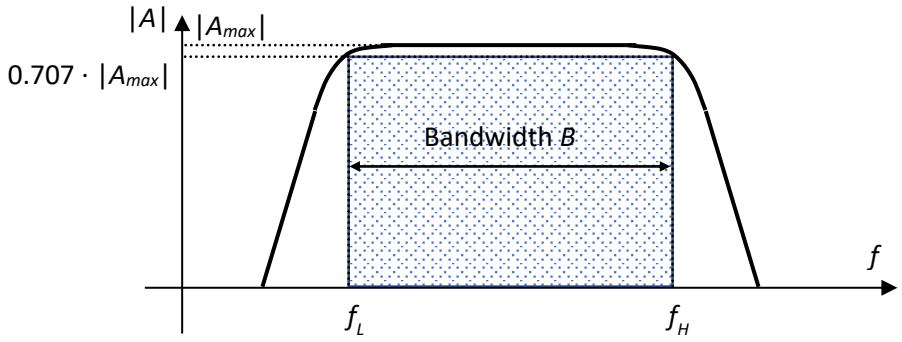


Fig.3.6. Gain-frequency plot of an amplifier

The bandwidth B is the difference between the high and low cut-off frequencies:

$$B = f_H - f_L$$

The two cut-off frequencies are obtained at a 3 dB attenuation of the maximum gain expressed in dB ((or 0.707 times the linear gain), and the signal is said to be inside the bandwidth when the frequency is within $[f_L; f_H]$. If the frequency is within $[f_L; f_H]$, the gain is assumed constant.

The conversion between the linear and the logarithmic scale (dB) of the gain is:

$$A_V[\text{dB}] = 20 \cdot log\,|A_V|$$
$$A_I[\text{dB}] = 20 \cdot log\,|A_I|$$
$$A_P[\text{dB}] = 10 \cdot log\,|A_P|$$

An amplifier behaves as a bandpass filter when using the capacitive coupling between consecutive stages. For integrated amplifiers, the amplifier stages are directly coupled, which leads to a lowpass filter behaviour, in the frequency domain.

Regardless of the capacitive or direct coupling between consecutive stages, the bandwidth of the amplifier must be known before using the amplifier in a circuit. For frequencies outside the band, amplifiers will additionally attenuate and introduce phase shifts in the output signals.

The gain-bandwidth product GBW is computed as the product of the gain and the frequency band for which the output is not attenuated and there is no phase shift.

$$GBW = |A| \cdot B \approx \text{constant}$$

The gain-bandwidth product GBW is given in the datasheet of any electronic device that has gain as one of its parameters.

Example

Determine five possible scenarios in which an amplifier with GBW = 200 kHz can be used.

Solution:

i) Gain A = 2, bandwidth B = 100 kHz
ii) Gain A = 5, bandwidth B = 40 kHz
iii) Gain A = 10, bandwidth B = 20 kHz
iv) Gain A = - 25, bandwidth B = 8 kHz
v) Gain A = 160, bandwidth B = 1.25 kHz.

3.5 Modelling electronic amplifiers

Electronic amplifiers deliver a greater output power than what was drawn from the input source and the power supplies. For signal variations, an electronic amplifier is modelled using a controlled source (*CS*). Controlled sources are pseudo-sources used to model the behaviour of active electronic devices (transistors, operational amplifiers) or active circuits (amplifiers). Devices modelled using controlled sources absorb power from the power supplies (dc power) and convert it into power for the variable output signal.

Controlled sources are active two-port networks for which the transfer parameter between input and output (i.e., the gain) is finite and not null. The output of controlled sources depends (is controlled) by the circuit connected at the input. The input represents the command (control) signal, while the output is the controlled signal.

The relation between the command signal and the controlled signal is linear (non-linear), and in this case the controlled source is also linear (non-linear). Electronic amplifiers are modelled using linear controlled sources. Based on the type of the controlled signal, there are voltage (Fig.3.7. a) or current controlled linear sources (Fig.3.7. b).

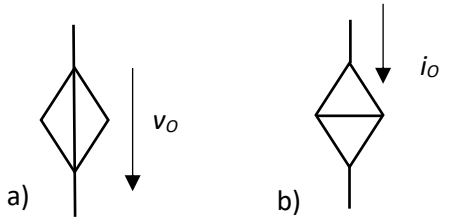


Fig.3.7. Symbols for controlled sources
a) voltage controlled source *VCS*;
b) current controlled source *CCS*.

For the complete modelling of an electronic amplifier, the input and output resistances must also be included. The models of the four types of amplifiers are shown in Fig.3.8. The input and output resistances of an amplifier become important when the amplifier is connected in a real signal processing chain, like the one shown in Fig.3.9. Here, a voltage source is connected at the input, and a load resistance at the output.

Two resistive dividers are formed, one at the input, between R_s and R_i, the other at the output, between R_o and R_L.

$$v_I = \frac{R_i}{R_i + R_s} \cdot v_S$$

$$v_O = \frac{R_L}{R_L + R_o} \cdot A_V \cdot v_I$$

The final expression of the output voltage is:

$$v_O = \frac{R_L}{R_L + R_o} \cdot \frac{R_i}{R_i + R_s} \cdot v_S \cdot A_V$$

To obtain a voltage that is not artificially attenuated, the two ratios must be as close to 1 as possible.

$$\frac{R_i}{R_i + R_s} \approx 1$$

$$\frac{R_L}{R_L + R_o} \approx 1$$

The ideal values of the input and output resistances are:

$$R_i >> R_s,\ R_i \rightarrow \infty$$

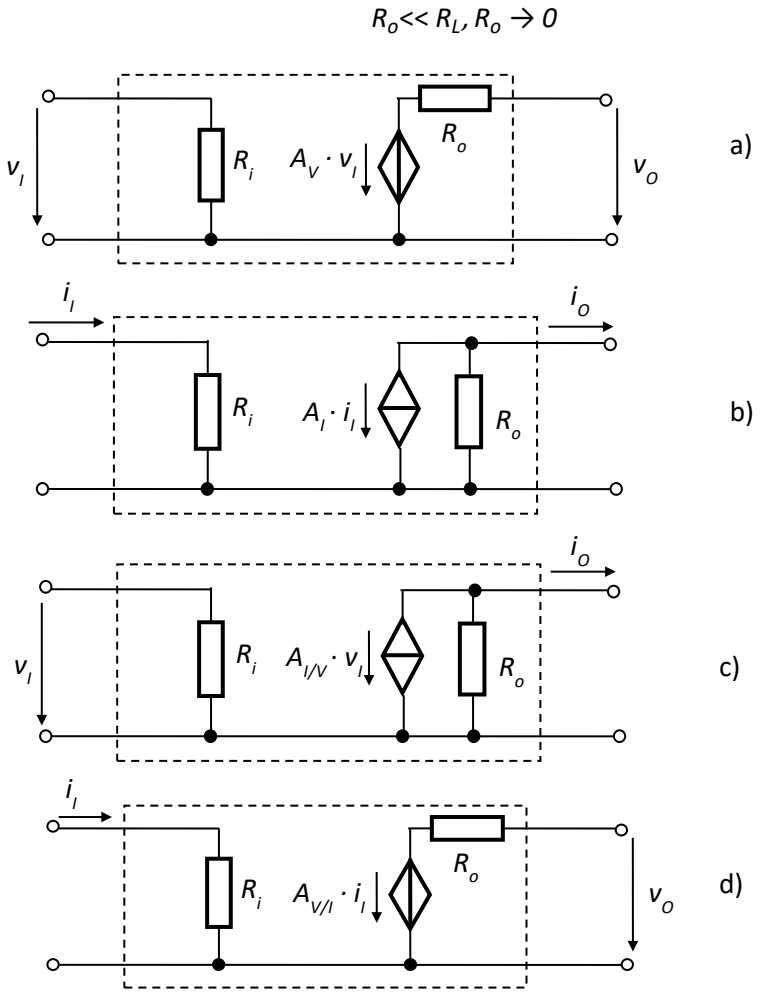


Fig.3.8. Modelling electronic amplifiers
a) voltage amplifier; b) current amplifier;
c) transconductance amplifier; d) trans-resistance amplifier.

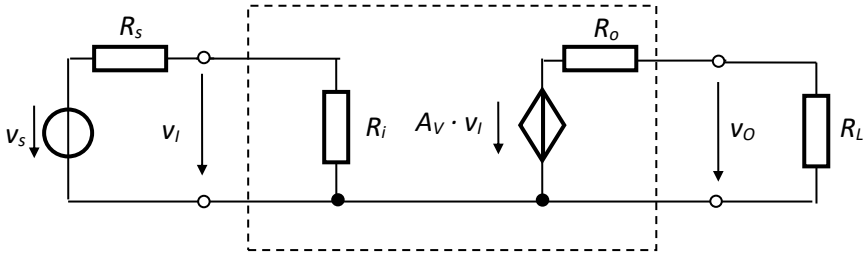


Fig.3.9. Amplifier with input voltage source and load resistance

The gain of the entire circuit is closer to the ideal value when the input resistance is as big as possible (ideally, infinite), and the output resistance is as small as possible (ideally zero). The ideal values of R_i and R_o for the four amplifiers are given in Table 3.1.

Table 3.1. Gain and ideal values for R_i R_o

Type of amplifier	Gain	R_i and R_o
Voltage	$A_V = \frac{v_O}{v_I}$	$R_i = \infty$ $R_o = 0$
Current	$A_i = \frac{i_O}{i_I}$	$R_i = 0$ $R_o = \infty$
Transconductance	$A_{i/v} = \frac{i_O}{v_I}$	$R_i = \infty$ $R_o = \infty$
Transresistence	$A_{v/i} = \frac{v_O}{i_I}$	$R_i = 0$ $R_o = 0$

3.6 Voltage transfer characteristics

For electronic amplifiers, the transfer characteristic depends on the gain (positive, negative) and the type of supplies (unipolar, differential).

A voltage amplifier with differential supply $\pm V_{PS}$ is shown in Fig.3.10, assuming ideal values for R_i and R_o.

The VTC $v_O(v_I)$ is depicted in Fig.3.11, where the linear relation between $v_O(t)$ and $v_I(t)$ is visible. The output voltage is limited to V_{OH} (upper limit) and V_{OL} (lower limit). For rail-to-rail amplifiers (which are more precise and thus more expensive circuits), $V_{OH} = +V_{PS}$ and $V_{OL} = -V_{PS}$; for common amplifiers, there will be a 1 ÷ 2 V difference between the values of the power supplies and the extreme values of the output voltage.

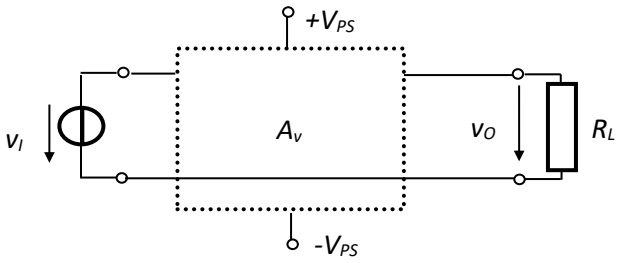


Fig.3.10. Voltage amplifier with differential supply

The range of values for which the amplifier works in the active region is:

$$v_I \in [V_{IL}, V_{IH}]$$

$$V_{IL} = \frac{V_{OL}}{A_V}$$

$$V_{IH} = \frac{V_{OH}}{A_V}$$

The active region is directly influenced by the gain. When the input voltage is outside the active region, the output is limited. If the power supplies don't change, the active region becomes narrower when the gain increases.

Sample waveforms for $v_I(t)$ and $v_O(t)$ are shown in Fig.3.12, where in Fig.3.12. a) the amplifier works in the active region, while in Fig.3.12. b), the amplifier works in both the active and the passive regions (output voltage is limited).

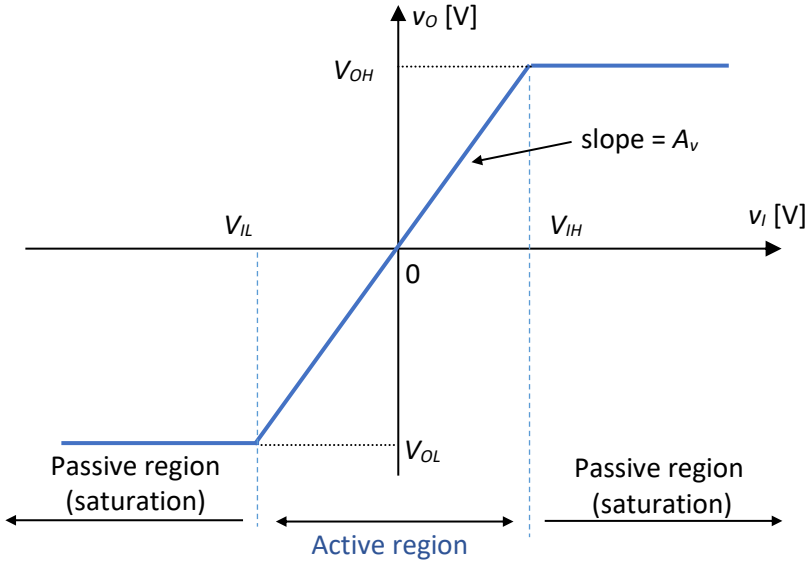


Fig.3.11. VTC $v_O(v_I)$ for the voltage amplifier with differential supply

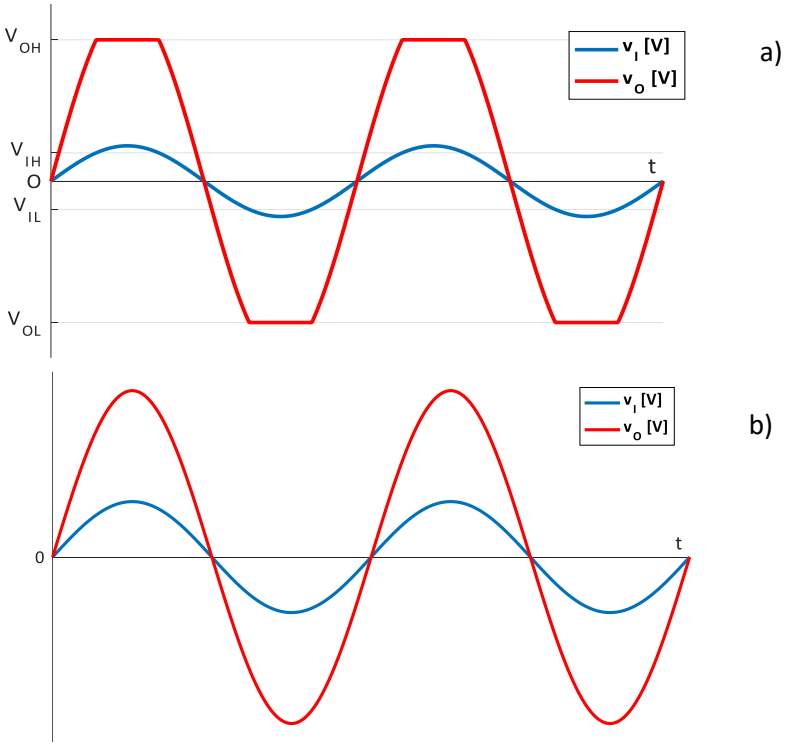


Fig.3.12. Waveforms for $v_I(t)$ and $v_O(t)$ for the voltage amplifier with differential supply a) active region; b) active and passive regions.

For amplifiers with differential supply, the output voltage can be positive and negative, there is no need for additional bias.

For amplifiers with unipolar supply, if the supply is positive, the output is limited to $V_{OH} \approx V_{PS}$ and $V_{OL} \approx 0$ V. In this case, for an input that is both positive and negative, only half the signal will be amplified. To amplify the entire signal, a bias dc voltage source V_{BIAS} is added, in series with the input (Fig.3.13).

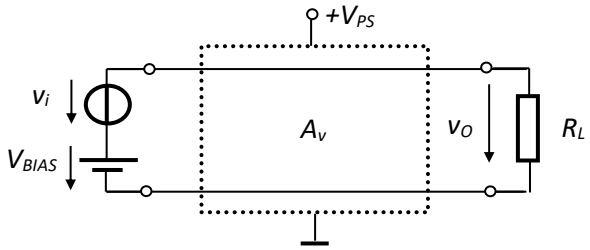


Fig.3.13. Voltage amplifier with unipolar supply and V_{BIAS}

By adding V_{BIAS}, the amplifier is biased in a quiescent point $Q(V_{BIAS}, V_O)$ located (ideally) in the middle of the active region. The signal at the input of the amplifier has both an ac component and a dc component:

$$v_I(t) = V_{BIAS} + v_i(t)$$

The output signal is also a sum between ac and dc components. The dc component V_O is the voltage in the quiescent point, as an effect of V_{BIAS}, and the ac component $v_o(t)$ is obtained by amplifying $v_i(t)$:

$$v_O(t) = V_O + v_o(t)$$
$$V_O = f(V_{BIAS})$$
$$v_o(t) = A_v \cdot v_i$$

The VTC $v_O(v_I)$ for the voltage amplifier with unipolar supply and V_{BIAS} is shown in Fig.3.14, and sample waveforms are depicted in Fig.3.15.

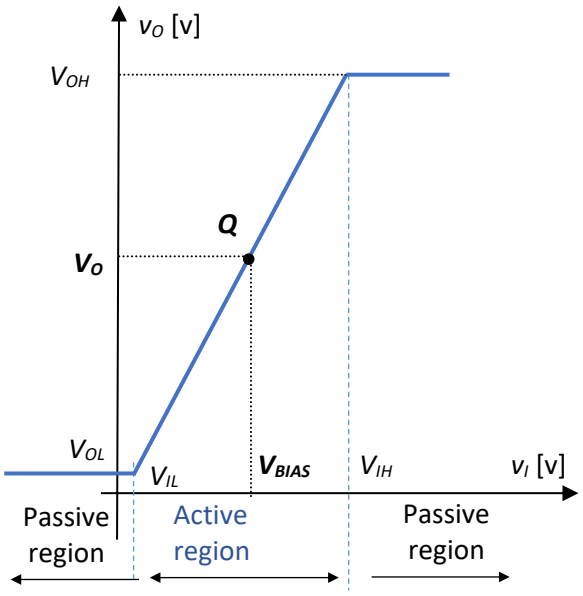


Fig.3.14. VTC $v_O(v_I)$ for the voltage amplifier with unipolar supply

The range of values for which the amplifier with unipolar supply works in the active region is:

$$v_I \in [V_{IL}, V_{IH}]$$

$$V_{IL} = \frac{V_{OL}}{2 \cdot A_V} \approx 0 \text{ V}$$

$$V_{IH} = \frac{V_{OH}}{2 \cdot A_V}$$

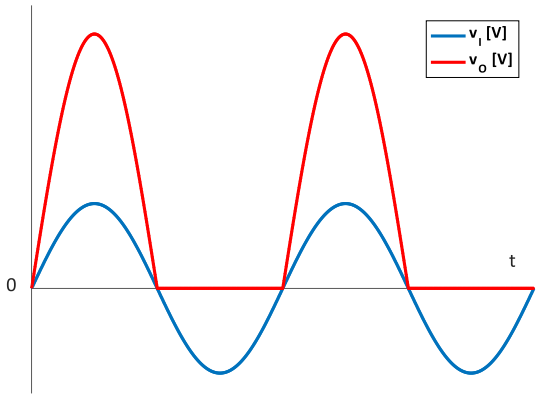


Fig.3.15. Waveforms of $v_I(t)$ and $v_O(t)$ for the voltage amplifier with unipolar supply in the active region

Examples

1. Compute the output voltage $v_o(t)$ for a differential amplifier with $A_v = 14$, $v_i(t) = 20\sin\omega t$ [mV][Hz].

Solution:

$$v_o(t) = A_v \cdot v_i(t)$$
$$v_o(t) = 14 \cdot 20\sin\omega t \text{ [mV][Hz]}$$
$$v_o(t) = 0.28\sin\omega t \text{ [V][Hz]}$$

2. Compute the active region for the amplifier in **Problem 1**, if the supplies are ±21 V.

Solution:

$$v_I \in \left[\frac{V_{OL}}{A_V}; \frac{V_{OH}}{A_V}\right]$$
$$v_I \in \left[\frac{-21}{14}; \frac{21}{14}\right] \text{ [V]}$$
$$v_I \in [-1.5;\ 1.5] \text{ [V]}$$

3. Determine the expressions of the input and output voltages for a voltage amplifier with unipolar supply, with $A_v = 14$, $v_i(t) = 20\sin\omega t$ [mV][Hz], $+V_{PS} = 15$ V, biased in the quiescent point Q, with $V_{BIAS} = 4$V and $V_O = 7.5$ V. Plot $v_I(t)$ and $v_O(t)$.

Solution:

$$v_O(t) = V_O + v_o(t)$$
$$v_I(t) = V_{BIAS} + v_i(t)$$
$$v_I(t) = 4 + 0.02\sin\omega t \text{ [V][Hz]}$$
$$v_o(t) = A_v \cdot v_I(t)$$
$$v_o(t) = 14 \cdot 20\sin\omega t \text{ [mV][Hz]}$$
$$v_o(t) = 0.28\sin\omega t \text{ [V][Hz]}$$
$$v_O(t) = 7.5 + 0.28\sin\omega t \text{ [V][Hz]}$$

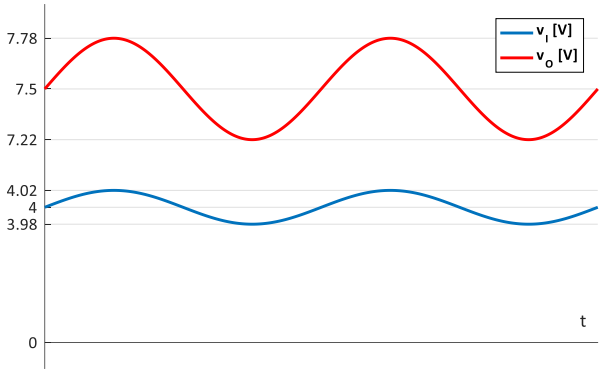


Fig.3.17. Waveforms for $v_I(t)$ and $v_O(t)$

Chapter 4

OPERATIONAL AMPLIFIERS

In this chapter, you will learn:

- the terminals and operation of the op-amp
- the behaviour of the op-amp in the active region and in saturation
- the analysis of circuits with op-amp as a comparator
- applications of comparators with op-amp
- the analysis of circuits with op-amp as an amplifier
- the non-ideal performance of op-amps
- applications of op-amps with negative feedback.

****

4.1 Introduction

The Operational Amplifier (OA or OpAmp or op-amp) is an integrated circuit, whose properties are very close to an those of an ideal electronic amplifier. The op-amp is made of active (transistors) and passive components (resistors and usually a capacitor), connected in a complex structure. The op-amp will be analysed as a device or building block, without going into details regarding its internal structure. The focus is on its terminal characteristics and typical applications.

Op-amps are highly versatile and are present in almost any electronic circuit. Depending on the application, a designer chooses from a wide variety of op amps, each designed for a specific purpose: high gain, high speed, thermal stability, low noise, low power consumption, rail-to-rail, low cost, low power supplies.

One of the most used op-amps, UA741, consists of 24 transistors, 12 resistors and a capacitor, integrated on the same silicon chip. The UA741 is available in metal or plastic cases, with 8, 14 or 16 terminals. The integrated circuit is implemented using THT (*Through Hole Technology*), as shown in Fig.4.1. a), or SMT (*Surface Mount Technology*) – Fig.4.1. b). For the UA741 in the 8 terminals case, the

dimensions of the case (length x width x height) are 10 x 8.5 x 5 mm for THT, and 5 x 6 x 1.75 mm for SMT.

Integrated circuits built using Through Hole Technology are connected on a PCB *Printed Circuit Board*) by inserting the terminals into holes and soldering on the opposite side. Integrated circuits built using Surface Mount Technology are soldered directly on the main side of the PCB. Integrated circuits and other components aimed to be soldered on the main side of the PCB are called *Surface Mount Devices* (SMD). SMDs have gradually replaced THT components in industrial fabrication, due to their reduced size and the ability to automate the soldering process.

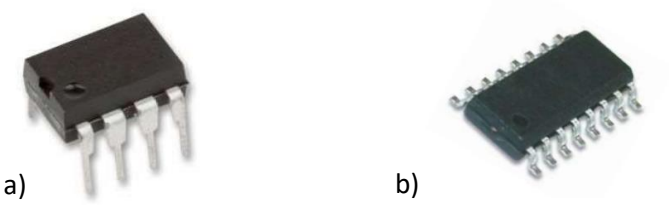


Fig.4.1. OA integrated circuit
a) 8 terminals, THT ; b) 16 terminals, SMT.

4.1.1 Op-amp terminals

The op-amp terminals are inputs, output, and supplies, as shown in Fig.4.2. The input terminals are called *noninverting input,* denoted v^+, and *inverting input,* denoted v^-. The supply terminals are denoted $+V_{PS}$, for the positive power supply, and $-V_{PS}$, for the negative power supply. Although sometimes the supply terminals are omitted from the schematics, and only the input and output terminals are shown, one must also assume a correct supply of the IC.

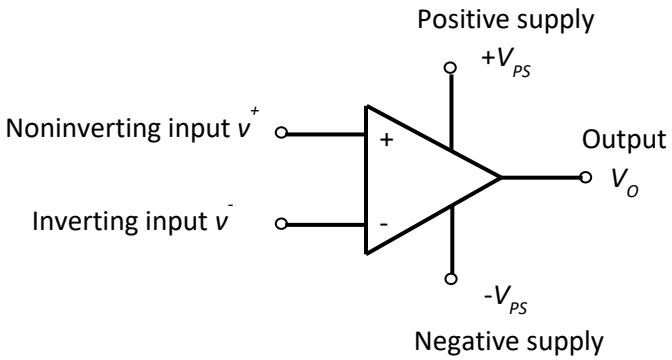


Fig.4.2. Op-amp terminals

The voltages applied at the input and supply terminals have one wire connected to ground, and any voltage in the circuit, including the output voltage, is measured with respect to this ground (0 V). The voltages applied at the two input terminals must be in the range determined by the two power supplies, for a proper functioning of the op-amp.

Symmetric differential supplies are commonly used for IC op-amps (the two dc voltage sources have the same absolute value). When one of the supplies is connected to ground (unipolar supply), the op-amp needs external biasing circuits (as discussed in Chapter 3), so that both the positive and the negative half-waves of the input are amplified.

Op-amps are *directly coupled amplifiers* or *dc amplifiers*, thus exhibiting a low-pass frequency characteristic.

4.1.2 Op-amp operation

The output voltage of an op-amp is a function of the *differential voltage* v_D and the *open loop gain*, denoted a (Fig.4.3). The currents absorbed by the two inputs of the op-amp are considered null (no current consumption).

$$v_O = a \cdot v_D$$

$$v_D = v^+ - v^-$$

$$i^+ = i^- = 0 \text{ mA}$$

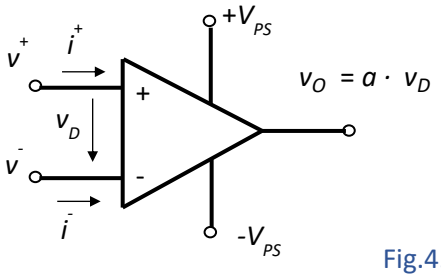


Fig.4.3. Op-amp operation

The op-amp can be modelled using a voltage-controlled voltage source, with the input v_D, as shown in Fig.4.4. The op-amp is close to an ideal amplifier when it comes to properties:

- high gain, $a \rightarrow \infty$
- high input resistance, $r_i \rightarrow \infty$, which implies no current consumption on the two inputs $i^+ = i^- = 0$ mA
- low output resistance, $r_o = 0$, which implies that the output voltage is independent of the load current
- high bandwidth, $B \rightarrow \infty$, which results in constant gain, regardless of the frequency of the input signal.

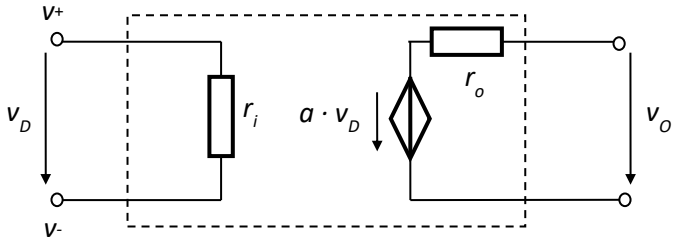


Fig.4.4. Modeling the op-amp with a voltage-controlled voltage source

Since the gain is high, ideally infinite, the output voltage becomes:

$$v_O = \infty \cdot v_D$$

This equation gives the two possible modes of operation for op-amps, as a switch and as an amplifier.

Op-amp as a switch

The electrical function of the op-amp when used as a switch is *voltage comparator.*

$$v_D > 0,\ v_O = +\infty$$
$$v_D < 0,\ v_O = -\infty$$

The output voltage cannot exceed the values imposed by the two power supplies, and it will be limited to V_{OH} (upper limit) and V_{OL} (lower limit). For rail-to-rail op-amps, $V_{OH} = +V_{PS}$ and $V_{OL} = -V_{PS}$.

$$v_O = \begin{cases} V_{OH}, & v_D > 0,\ v^+ > v^- \\ V_{OL}, & v_D < 0,\ v^+ < v^- \end{cases}$$

The output voltage switches between the two extreme values when the differential voltage $v_D = 0$.

Op-amp as an amplifier

To use the op-amp for voltage amplification, the differential voltage v_D must always be kept at 0 V, by means of an external circuit. The output voltage then becomes $v_O = \infty \cdot 0$, an indeterminate form which results in $v_O \in [V_{OL}; V_{OH}]$.

$$v_D = 0,\ v_O = \infty \cdot 0 = \text{constant}$$
$$v_O \in [V_{OL}; V_{OH}]$$

The differential voltage v_D is kept at 0 V by adding a negative feedback loop in the circuit (connection between output and inverting input of the op-amp).

4.2 Voltage comparators with op-amp

When using the op-amp as a switch (in switching mode) the output voltage switches between the two extreme values, V_{OL} and V_{OH}. The circuits in which the op-amp works as a switch are called *voltage comparators.* A voltage comparator is a circuit that signalizes the relative state of two input voltages (v^+ and v^-), through two different states of the output voltage. For op-amp comparators, the input is the differential voltage $v_D = v^+ - v^-$.

$$v_O = \begin{cases} V_{OH}, & v_D > 0,\ v^+ > v^- \\ V_{OL}, & v_D < 0,\ v^+ < v^- \end{cases}$$

The VTC $v_O(v_D)$ of an ideal op-amp, with v_D as input and v_O as output, is depicted in Fig.4.5. The op-amp is considered rail-to-rail:

$$V_{OH} = +V_{PS},\ V_{OL} = -V_{PS}$$

Two types of voltage comparators can be built using op-amps: simple comparators and positive feedback (hysteresis) comparators. For all circuits discussed in this chapter, the op-amps are considered rail-to-rail.

4.2.1 Simple comparators

A simple comparator is obtained when using the op-amp without feedback. In electronic circuits, a feedback loop is a backward connection, from output to input. By using feedback loops, the input is influenced by the output. It is common to use variable signals for one of the op-amp's inputs, and a dc voltage source or even connection to ground, for the remaining input. Two simple comparators are shown in Fig.4.6: a) v_I applied to the noninverting input, and b) v_I applied to the inverting input.

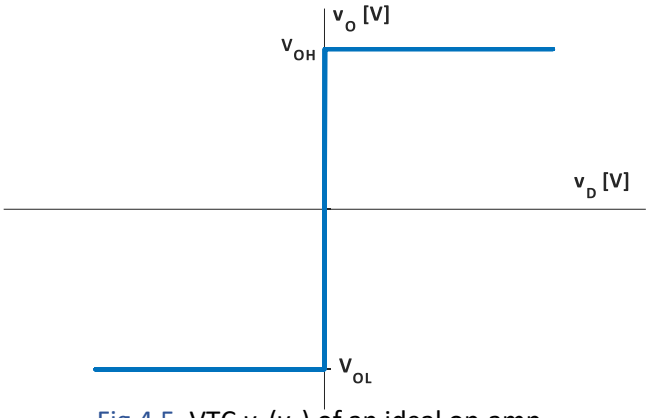


Fig.4.5. VTC $v_O(v_D)$ of an ideal op-amp

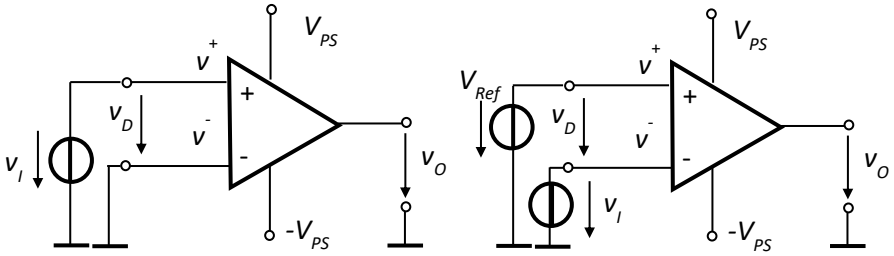


Fig.4.6. Simple comparators with op-amp: a) $v_I = v^+$; b) $v_I = v^-$.

Judging by the input of the op-amp to which the variable voltage v_I is applied, comparators are categorized into:

- *noninverting comparators*, v_I goes to v^+, either directly or by means of other components, Fig.4.6. a)
- *inverting comparators*, v_I goes to v^-, either directly or by means of other components, Fig.4.6. b).

The particular, special value of v_I for which the output voltage v_O switches between the two extreme values V_{OL} and V_{OH} is called the *threshold voltage* of the comparator, denoted V_{Th}. The output switches when $v_D = 0$ V.

$$V_{Th} = v_I|_{v_D = 0}$$

Based on the value of the threshold voltage, there are comparators with $V_{Th} = 0$ V, as well as comparators with $V_{Th} \neq 0$ V.

Comparators with $V_{Th} = 0$ V

These are the simplest voltage comparators with op-amp. A zero-threshold voltage means that the "free" input of the op-amp is grounded. The circuit in Fig.4.6. a) is a noninverting voltage comparator, with $V_{Th} = 0$ V.

The VTC $v_O(v_I)$ is determined by replacing the values of v^+ and v^- in the equation of the op-amp. For the circuit in Fig.4.6. a), the equations are:

$$v^+ = v_I$$
$$v^- = 0 \text{ V}$$
$$v_D = v_I$$

$$v_O = \begin{cases} V_{OH}, & v_D > 0, \; v^+ > v^-, v_I > 0 \text{ V} \\ V_{OL}, & v_D < 0, \; v^+ < v^-, v_I < 0 \text{ V} \end{cases}$$

When the input voltage is above 0 V, the output is maximum, while for the input below 0 V, the output is minimum. In other words, a high input determines a high output, a low input determines a low output, hence the noninverting character of the comparator.

The VTC $v_O(v_I)$ of the simple comparator, noninverting, with V_{Th} = 0 V is shown in Fig.4.7. a), and sample waveforms for $v_I(t)$ and $v_O(t)$ are presented in Fig.4.7. b). The VTC $v_O(v_I)$ is in the 1st and 3rd quadrants, and the input and output voltages are in phase. The threshold voltage can be deduced from the VTC $v_O(v_I)$, as being the particular value of v_I for which the output voltage switches.

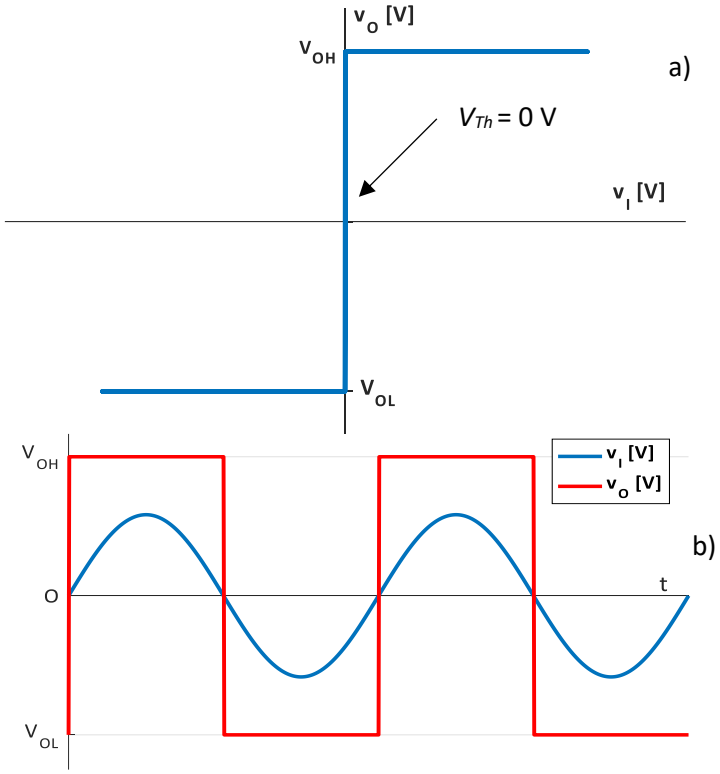


Fig.4.7. Simple comparator, noninverting, V_{th} = 0 V
a) VTC $v_O(v_I)$; b) waveforms for $v_I(t)$ and $v_O(t)$.

To obtain a simple inverting comparator with with V_{Th} = 0 V, a switch must be done between the voltages applied at the inputs of the op-amp. The input voltage is now connected to the inverting input (hence the inverting character of the comparator), while the noninverting input is grounded, as seen in Fig.4.8 a).

$$v^+ = 0 \text{ V}$$
$$v^- = v_I$$
$$v_D = - v_I$$

$$v_O = \begin{cases} V_{OH}, & v_D > 0, \; v^+ > v^-, v_I < 0 \text{ V} \\ V_{OL}, & v_D < 0, \; v^+ < v^-, v_I > 0 \text{ V} \end{cases}$$

The VTC $v_O(v_I)$ is depicted in Fig.4.8. b). The VTC is in the 2nd and 4th quadrants. Sample waveforms for $v_I(t)$ and $v_O(t)$ are shown in Fig.4.9. The input and output voltages are in anti-phase (a low input determines a high output, and vice versa).

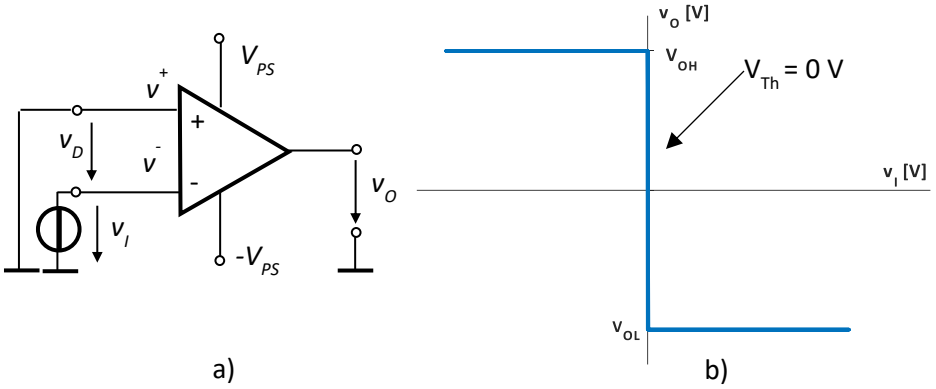


Fig.4.8. Simple inverting comparator with with V_{Th} = 0 V: a) circuit;) VTC $v_O(v_I)$.

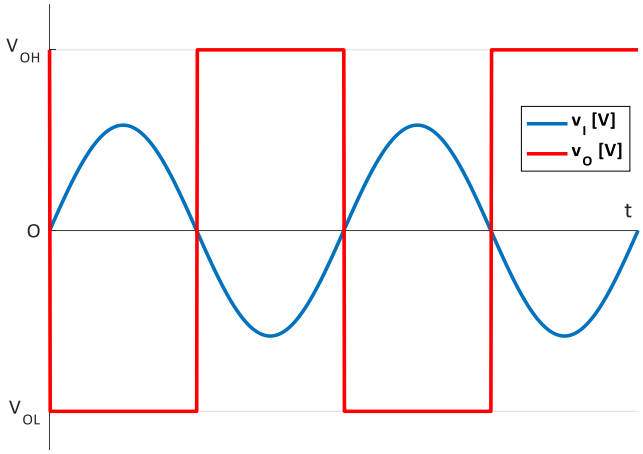


Fig.4.9. Simple inverting comparator - waveforms for $v_I(t)$ and $v_O(t)$

Comparators with $V_{Th} \neq 0$ V

There are cases when the input voltage needs to be compared to a non-zero reference value, denoted V_{Ref}. These circuits are also simple comparators, and, based on the terminal to which the input voltage is connected, can be inverting or noninverting.

A simple comparator, noninverting, with $V_{Th} \neq 0$ V is shown in Fig.4.10, and its VTC $v_O(v_I)$ is in Fig.4.11. a), along with sample waveforms for $v_I(t)$ and $v_O(t)$ in Fig.4.11. b). The extreme values of the VTC are still in the 1st and 3 quadrants (noninverting), and, for the chosen example, the threshold

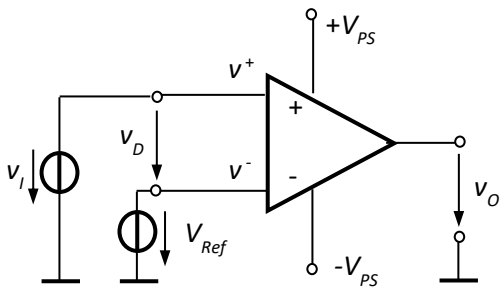


Fig.4.10. Simple comparator, noninverting, with $V_{Th} \neq 0$ V

voltage is positive. The input and output voltages are in phase, but this time, the output voltage no longer switches at 0 V, but at a positive value.

The equations of the circuit are:

$$v^+ = v_I$$
$$v^- = V_{Ref}$$
$$v_D = v_I - V_{Ref}$$
$$V_{Th} = v_I|_{v_D = 0}$$

When $v_D = 0$, the threshold voltage is $V_{Th} = V_{Ref}$

$$v_O = \begin{cases} V_{OH}, & v_D > 0, \; v^+ > V_{Ref}, \; v_I > V_{Ref} \\ V_{OL}, & v_D < 0, \; v^+ < V_{Ref}, \; v_I < V_{Ref} \end{cases}$$

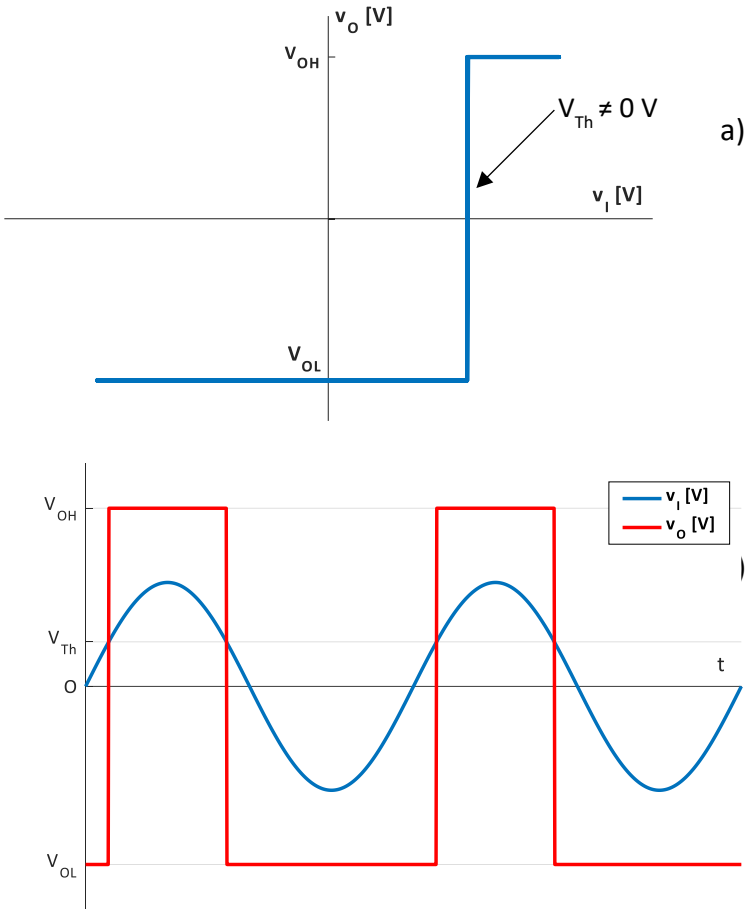


Fig.4.11. Simple comparator, noninverting, $V_{Th} \neq 0$ V
a) VTC $v_O(v_I)$; b) waveforms for $v_I(t)$ and $v_O(t)$.

The reference voltage V_{Ref} which gives the threshold of the comparator is usually obtained from the dc supplies of the op-amp, and thus $V_{Ref} \in [-V_{PS}; +V_{PS}]$. The easiest way of obtaining a non-zero threshold voltage is to use a voltage divider, i.e. resistors connected between the dc supply and the input of the op-amp. For a positive V_{Ref}, the resistive divider is connected to $+V_{PS}$ (see Fig.4.12), while for negative V_{Ref}, the resistive divider is connected to $-V_{PS}$.

For the circuit in Fig.4.12, the same current, coming from $+V_{PS}$, goes through both resistors (the resistors are in series, since ($i^- = 0$).

The reference voltage V_{Ref} is the voltage drop across resistor R_1 and computed as:

$$V_{Ref} = \frac{R_1}{R_1 + R_2} \cdot V_{PS}$$

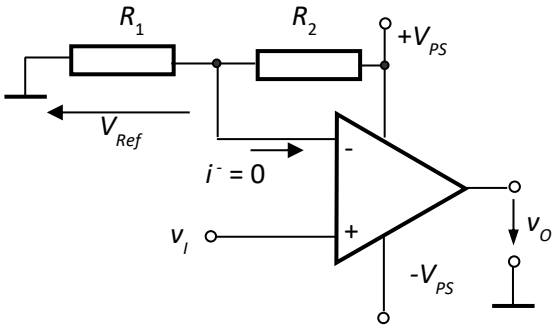


Fig.4.12. Simple comparator, noninverting, $V_{Th} \neq 0$ V, with resistive divider

A non-zero threshold voltage $V_{Th} \neq 0$ V can also be obtained using a potentiometer, a Zener diode in series with a resistor or a current source (to bias the Zener diode with the appropriate current).

An inverting simple comparator with $V_{Th} \neq 0$ V is shown in Fig.4.13. a), its VTC $v_O(v_I)$ is in Fig.4.13. b), along with sample waveforms for $v_I(t)$ and $v_O(t)$ in Fig.4.13. c).

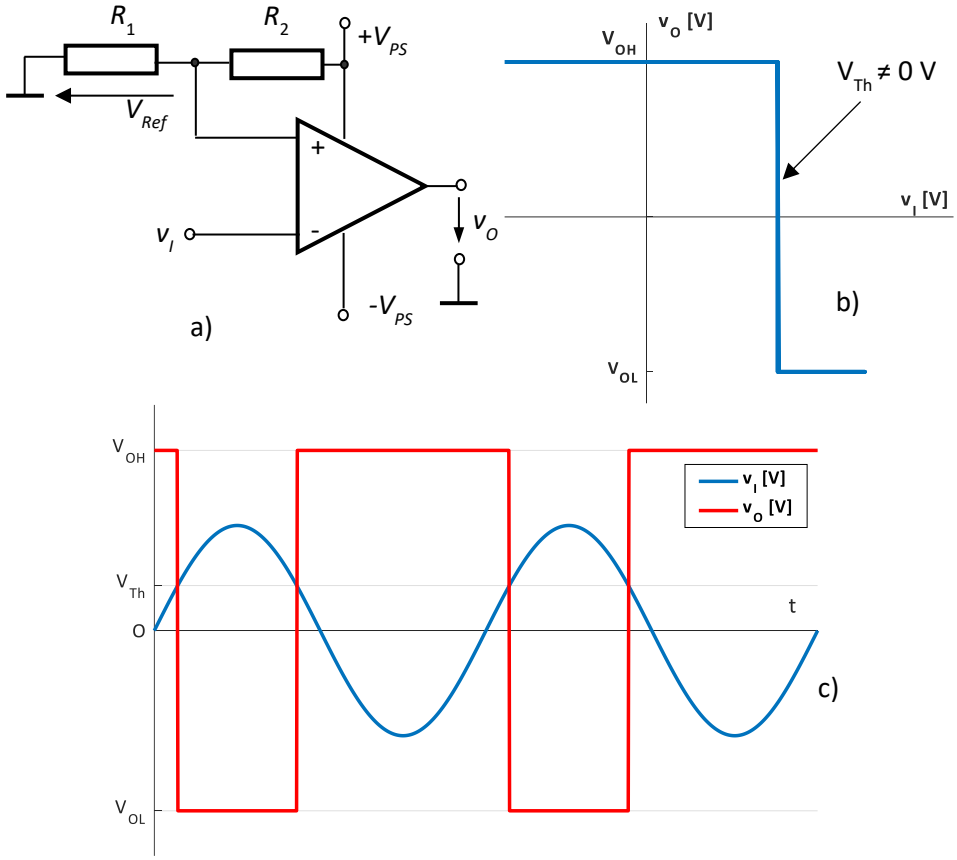


Fig.4.13. Simple comparator, inverting, $V_{Th} \neq 0$ V
a) circuit; b) VTC $v_O(v_I)$; c) waveforms for $v_I(t)$ and $v_O(t)$.

There are op-amps dedicated to being used as comparators: high speed (rapid switch between V_{PS} and $-V_{PS}$), additional external resistance, additional grounded terminal.

Example

Design and size a simple noninverting comparator with V_{Th} = -3V, differential supply of ± 12 V. Deduce and plot the VTC $v_O(v_I)$ for $v_I(t) = 8\sin\omega t$ [V][Hz]. Plot $v_I(t)$ and $v_O(t)$ for:
i) $v_I(t) = 2\sin\omega t$ [V][Hz]
ii) $v_I(t) = 5\sin\omega t$ [V][Hz].

Solution:

The proposed circuit is shown in Fig.4.14. The reference voltage, which also represents the threshold, is obtained using a resistive divider connected to the negative supply, because V_{Th} needs to be negative.

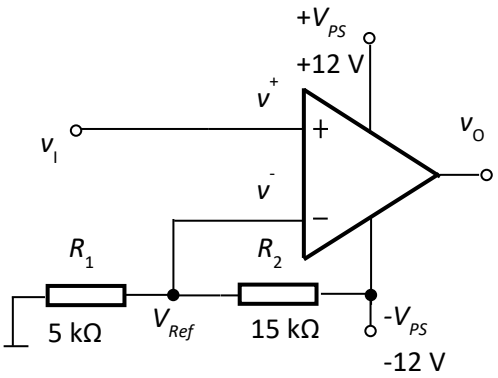


Fig.4.14. Simple noninverting comparator with negative threshold voltage

The circuit's equations are:

$$v^+ = v_I$$
$$v^- = V_{Ref}$$
$$v_D = v_I - V_{Ref}$$
$$V_P = v_I\,|_{v_D = 0}$$
$$V_P = V_{Ref}$$
$$V_{Ref} = \frac{R_1}{R_1 + R_2}\cdot(-V_{PS})$$
$$-3 = \frac{R_1}{R_1 + R_2}\cdot(-12)$$
$$\frac{R_1}{R_1 + R_2} = \frac{3}{12} = \frac{1}{4}$$
$$R_2 = 3\cdot R_1$$

Possible values for the two resistors are:

$$R_1 = 3\ \text{k}\Omega;\ R_2 = 9\ \text{k}\Omega$$
$$R_1 = 5\ \text{k}\Omega;\ R_2 = 15\ \text{k}\Omega$$

The VTC $v_O(v_I)$ is next deduced and plotted in Fig.4.15.

$$v_O = \begin{cases} V_{OH},\ v_D > 0,\ v^+ > V_{Ref},\ v_I > V_{Th} \\ V_{OL},\ v_D < 0,\ v^+ < V_{Ref},\ v_I < V_{Th} \end{cases}$$

$$v_O = \begin{cases} 12\ \text{V},\ v_D > 0,\ v^+ > V_{Ref},\ v_I > -3\ \text{V} \\ -12\ \text{V},\ v_D < 0,\ v^+ < V_{Ref},\ v_I < -3\ \text{V} \end{cases}$$

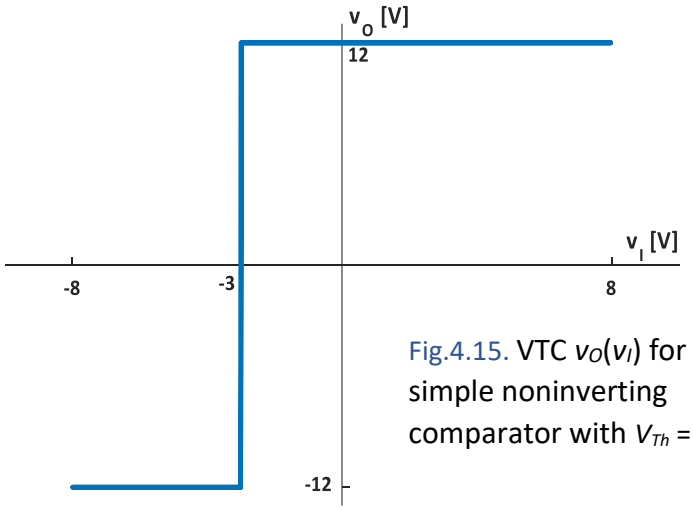


Fig.4.15. VTC $v_O(v_I)$ for the simple noninverting comparator with V_{Th} = -3 V

The output voltage $v_O(t)$ does not switch for the input voltage in i), because the input voltage is always above the threshold - Fig.4.16. a). For the input voltage in ii), the output switches between V_{OH} and V_{OL} each time the input voltage is equal to V_{Th} – Fig.4.16. b).

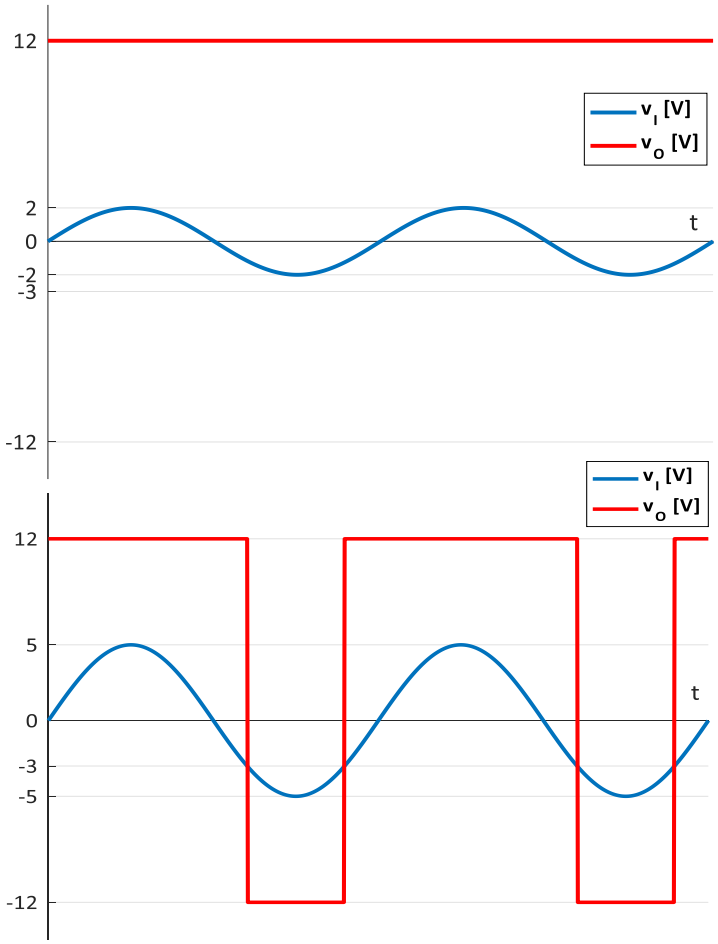


Fig.4.16. Waveforms for $v_I(t)$ and $v_O(t)$ for a) case i); b) case ii).

Problems
1. Design and size a noninverting simple comparator with V_{Th} = 0 V, differential supply of ± 15V. Deduce and plot the VTC $v_O(v_I)$ for $v_I(t)$ = 8sinωt [V][Hz]. Plot $v_I(t)$ and $v_O(t)$.
2. Design and size an inverting simple comparator with V_{Th} = 4 V, differential supply of ± 10V. Deduce and plot the VTC $v_O(v_I)$ for $v_I(t)$ = 8sinωt [V][Hz]. Plot $v_I(t)$ and $v_O(t)$.
3. Modify the circuit proposed at **Problem 2**, so that the threshold voltage becomes adjustable, $V_{Th} \in$ [-10 V; + 10 V].

4.2.2 Applications of simple comparators

Comparators with op-amp are used in logic circuits, circuits that interface between analog and digital stages, circuits that transform a sinusoidal or a triangular wave into a square (rectangular) wave, optical voltage level indicators, pulse-width modulation circuits, command and signalling circuits, analog-to-digital converters, etc.

Shaping a square wave from a sinusoidal (or triangular) wave

A square wave with adjustable duty cycle is obtained by using a simple comparator with adjustable threshold voltage, with a sinusoidal or triangular input - Fig.4.17. The duty cycle of the square output voltage is adjustable from 0% to 100%. The reference voltage is a function of the values of the resistors, value of the potentiometer, and the two power supplies:

$$V_{Ref} = \frac{k \cdot P + R}{P + 2 \cdot R} \cdot (+V_{PS}) + \frac{(1-k) \cdot P + R}{P + 2 \cdot R} \cdot (-V_{PS})$$

$$V_{Ref} = \frac{P \cdot (2 \cdot k - 1)}{P + 2 \cdot R} \cdot (+V_{PS})$$

$$k \in [0; 1]$$

$$V_{Ref} \in [\frac{P}{P + 2 \cdot R}(-V_{PS}); \frac{P}{P + 2 \cdot R} V_{PS}]$$

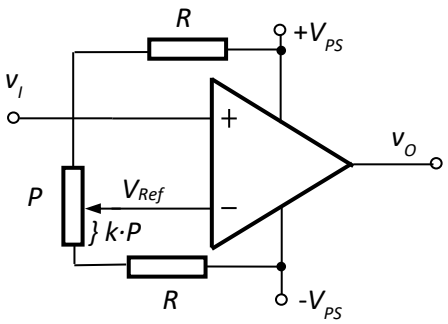


Fig.4.17. Circuit for obtaining a square wave from a sinusoidal wave

Sample waveforms for $v_I(t)$ and $v_O(t)$ are given in Fig.4.18, for two different values V_{Ref} (positive and negative). Note the change in the shape of the square signal, by examining the duty cycle.

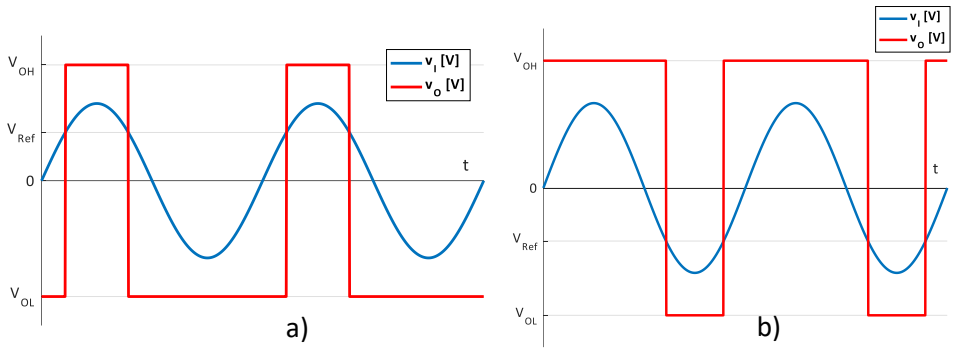


Fig.4.18. Waveforms for $v_I(t)$ and $v_O(t)$ for the circuit in Fig.4.17
a) $V_{Ref} > 0$; a) $V_{Ref} < 0$.

Optical voltage level indicator

One or more simple comparators with op-amp can be used to build an optical voltage level indicator. The example in Fig.4.19 has three noninverting comparators (same input voltage, connected to the noninverting input) and four LEDs. For the practical implementation of this circuit, IC324 is used. Each op-amp is ¼ of the IC324, which consists of 4 independent op-amps in a single chip.

The threshold voltages for each of the three simple comparators are obtained by means of the resistive network connected between +12 V and ground.

$$V_{Th1} = \frac{R_1}{R_1 + R_2 + R_3 + R_4} \cdot (+12\ \text{V})$$

$$V_{Th2} = \frac{R_1 + R_2}{R_1 + R_2 + R_3 + R_4} \cdot (+12\ \text{V})$$

$$V_{Th3} = \frac{R_1 + R_2 + R_3}{R_1 + R_2 + R_3 + R_4} \cdot (+12\ \text{V})$$

The output voltages are:

$$v_{O1} = \begin{cases} 12\ \text{V}, v_I > 2\ \text{V} \\ 0\ \text{V}, v_I < 2\ \text{V} \end{cases}$$

$$v_{O2} = \begin{cases} 12\ \text{V}, v_I > 4\ \text{V} \\ 0\ \text{V}, v_I < 4\ \text{V} \end{cases}$$

$$v_{O3} = \begin{cases} 12\ \text{V}, v_I > 6\ \text{V} \\ 0\ \text{V}, v_I < 6\ \text{V} \end{cases}$$

Table 4.1 synthesises the functioning of the circuit.

Table 4.1. Functioning of the optical voltage level indicator – one LED *on* at any given time

Range of v_I	***LED*$_1$**	***LED*$_2$**	***LED*$_3$**	***LED*$_4$**
[0 V; 2 V]	*on*	*off*	*off*	*off*
(2 V; 4 V]	*off*	*on*	*off*	*off*
(4 V; 6 V]	*off*	*off*	*on*	*off*
(6 V; 12 V]	*off*	*off*	*off*	*on*

Based on the value of the input voltage, the LEDs successively turn on. A single LED is *on* at any given time, based on the range of values of the input voltage. For example, if the input voltage is 3 V,

that is v_I belongs to (2 V; 4 V], LED_2 will be *on*, while the other three LEDs are *off*. The threshold values of the three op-amps determine the ranges for v_I. If other threshold values are required, the resistive divider R_1 to R_4 needs to be resized.

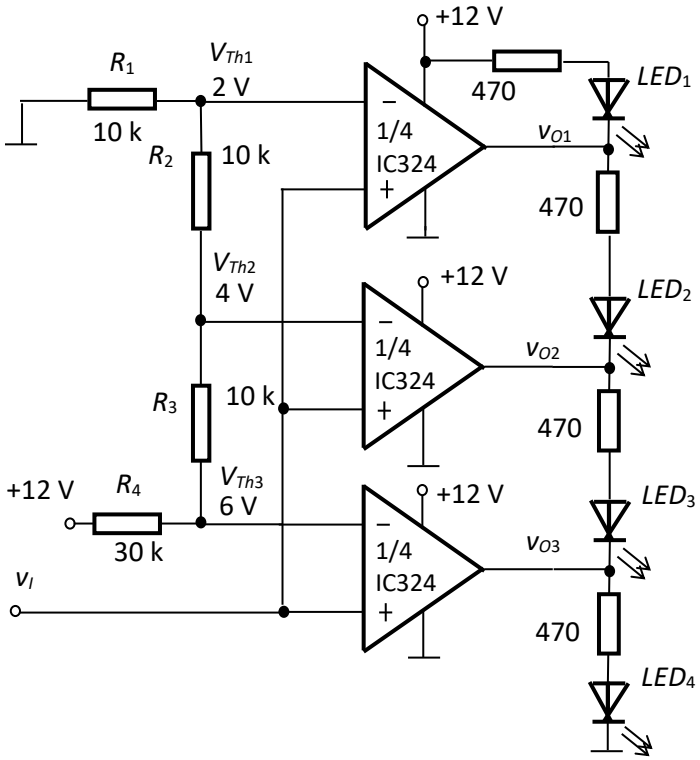


Fig.4.19. Optical voltage level indicator –one LED is *on* at any given time

Another type of optical voltage level indicator is the one where the LEDs gradually turn *on*, in accordance with the value of the input voltage. The bigger the input voltage, the more LEDs are *on.* Such a circuit is presented in Fig.4.20, with two op-amps and three *LED*s. The threshold voltages are V_{Th1} = 2.5 V, V_{Th2} = 6 V. Table 4.2 describes the functioning of the circuit.

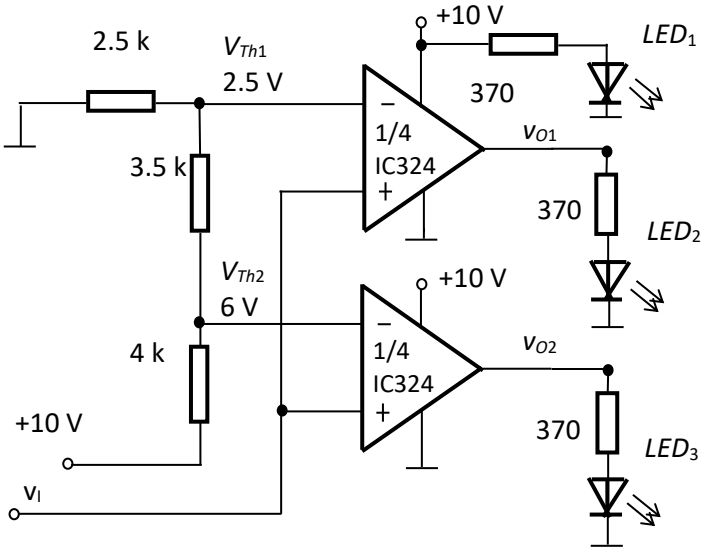


Fig.4.20. Optical voltage level indicator – LEDs gradually turn *on*

Table 4.2. Functioning of the optical voltage level indicator– LEDs gradually turn *on*

Range of v_I	***LED*$_1$**	***LED*$_2$**	***LED*$_3$**
[0 V; 2.5 V]	*on*	*off*	*off*
(2.5 V; 6 V]	*on*	*on*	*off*
(6 V; 10 V]	*on*	*on*	*on*

Pulse width modulation

Pulse width modulation is obtained when both signals applied at the inputs of the op-amp are variable, one is a sinewave – $v_{i1}(t)$, and the other a triangular wave – $v_{i2}(t)$, with a higher frequency (Fig.4.21. a). The information signal is the sinusoidal wave, $v_{i1}(t)$. The higher the frequency of the triangular wave, the lower the modulation errors. The period of the output rectangular voltage is that of the triangular wave, and the duty cycle is variable. The waveforms for $v_{i1}(t)$, $v_{i2}(t)$, and $v_o(t)$ are shown in Fig.4.21. b).

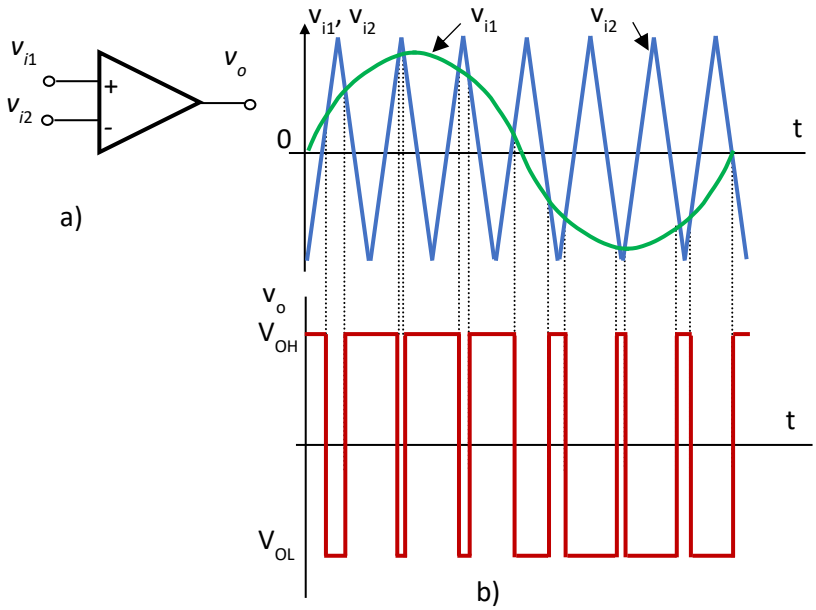


Fig.4.21. Pulse width modulation
a) circuit; b) waveforms for $v_{i1}(t)$, $v_{i2}(t)$, and $v_o(t)$ [2].

4.2.3 Hysteresis comparators

In a signal processing system, when the information signal is, often, affected by noise, simple comparators reveal their drawback: the output switches between V_{OH} and V_{OL} each time the signal meets the threshold voltage. The waveforms for $v_I(t)$ and $v_O(t)$ for a simple inverting comparator with $V_{Th} = 0$ V are shown in Fig. 4.22. a). The input voltage $v_I(t)$ is affected by noise and therefore intersects with the threshold voltage multiple times. Consequently, the output voltage exhibits unwanted, parasitic switches. The simple comparator instantly reacts (switches the output voltage) whenever the input meets the threshold.

The solution is to use a comparator with two threshold voltages, and the difference between the two thresholds must exceed the amplitude of the noise – Fig.4.22. b). At any given time, only one of

the two thresholds is active (determines a switch in the output voltage). The active threshold is based on the previous value of the output voltage.

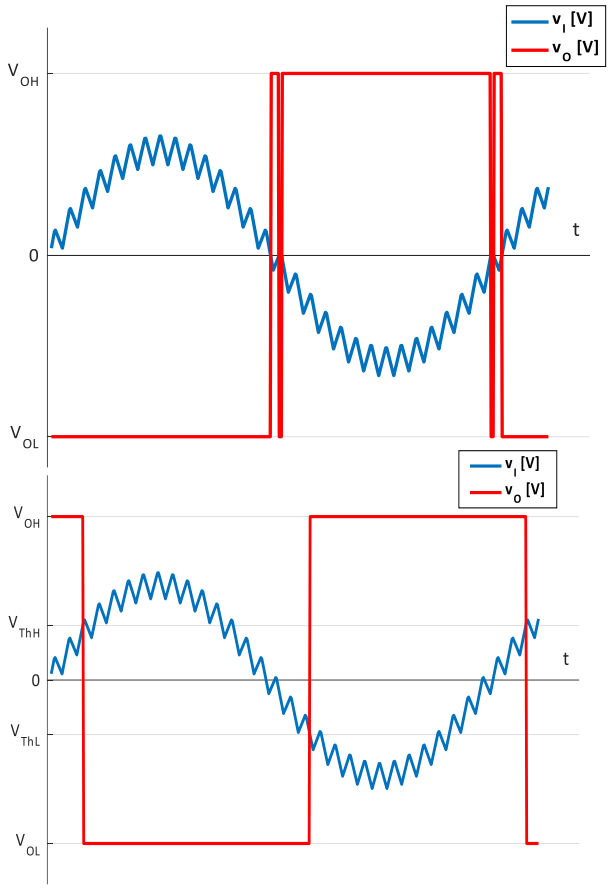


Fig.4.22. Waveforms for $v_I(t)$ and $v_O(t)$ for a noisy input
a) simple comparator, $V_{Th} = 0$ V – parasitic switches in the output voltage;
b) hysteresis comparator – no parasitic switches.

To obtain two threshold voltages, a part of the output is fed back into the op-amp, through the noninverting input. This mechanism is called *positive feedback*. Comparators with two threshold voltages, V_{ThH} and V_{ThL}, are called *positive feedback comparators* or *hysteresis comparators*. Hysteresis comparators can also be inverting or noninverting, based on the terminal to which the input voltage is connected.

Hysteresis comparator with symmetric threshold voltages

The positive feedback loop is obtained by means of a resistive divider between output and the noninverting input of the op-amp, as shown in Fig.4.23. The circuit is inverting (input goes to v^-) and the thresholds are symmetrical (with respect to 0 V).

The values of the threshold voltages are computed by using the same starting point as for simple comparators: the thresholds are particular values of v_I, when $v_D = 0$ V.

$$V_{Th} = v_I \big|_{v_D = 0}$$
$$v_D = v^+ - v^-$$

$$v^+ = \frac{R_1}{R_1 + R_2} \cdot v_O$$
$$v^- = v_I$$
$$v^+ = v^- \Rightarrow \frac{R_1}{R_1 + R_2} \cdot v_O = V_{Th}$$

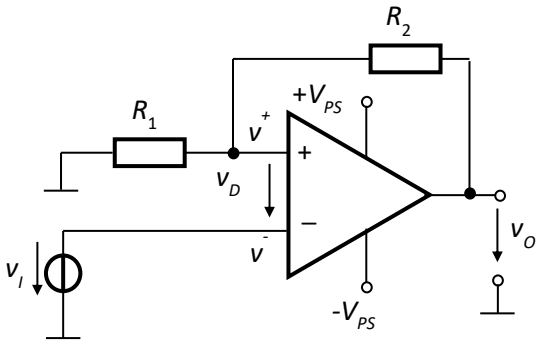


Fig.4.23. Hysteresis comparator, inverting, with symmetric threshold voltages

The threshold depends on the output voltage, and since there are only two possible values for the output voltage (V_{OH} and V_{OL}), there will be two different thresholds.

$$V_{ThH} = \frac{R_1}{R_1 + R_2} \cdot V_{OH}$$
$$V_{ThL} = \frac{R_1}{R_1 + R_2} \cdot V_{OL}$$

Two threshold voltages mean that, on the VTC $v_O(v_I)$ of the inverting hysteresis comparator (Fig.4.24. a), there will be two values of v_I for which the output v_O switches between its extreme values, V_{OH} and V_{OL}. This special shape of the VTC is called *hysteresis*, and it indicates a phenomenon according to which the current value of a quantity (material) also depends on previous values of other quantities determining it.

The two thresholds are symmetrical with respect to 0 V. When v_I is below the high threshold and it increases, the direction is left to right on the hysteresis (1 → 2 → 3, or clockwise), and the active threshold is V_{ThH}. In other words, the output is V_{OH} until v_I meets the high threshold, then switches to V_{OL}. When v_I decreases, the direction is right to left on the hysteresis (3 → 4 → 1), and the active threshold is V_{ThL}. In other words, the output is V_{OL} until v_I meets the low threshold, then switches to V_{OH}. A hysteresis comparator can be seen as a memory circuit: the active threshold is determined by the previous value of the output.

The distance between the two thresholds is called the *hysteresis width* and is always positive. The hysteresis width determines the comparator's immunity to noisy signals and is computed as:

$$\Delta V_{Th} = V_{ThH} - V_{ThL} = \frac{R_1}{R_1 + R_2} \cdot (V_{OH} - V_{OL})$$

Sample waveforms for $v_I(t)$ and $v_O(t)$ are shown in Fig.4.24. b). The input and output voltage exhibit a phase delay, but the inverting character of the comparator is still noticeable: high/low input determines a low/high output.

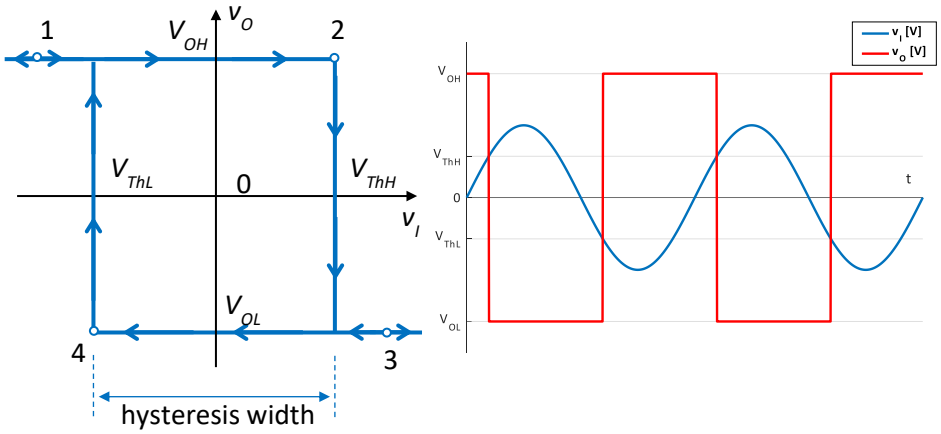


Fig.4.24. Hysteresis comparator, inverting, with symmetric threshold voltages
a) VTC $v_O(v_I)$; b) waveforms for $v_I(t)$ and $v_O(t)$.

Hysteresis comparators are bistable circuits, the two stable states of the output voltage are V_{OH} and V_{OL}. The circuit can remain in either state for an infinite time, if the input voltage does not change. The input voltage triggers the switch of the output voltage, and this switch is further sustained by means of the positive feedback. Hysteresis comparators are also known as *bistable multivibrator circuits* or *Schmitt triggers*.

A noninverting hysteresis comparator is obtained when the input voltage is connected to the noninverting input of the op-amp. Note that when going from inverting hysteresis comparator to noninverting hysteresis comparator, switching the inputs of the op-amp (inverting and noninverting) does not do the trick: the positive feedback loop must stay in place, so the viable solution is to just move the input voltage to the desired input, in this case the noninverting input.

The schematic for a noninverting hysteresis comparator with symmetric thresholds is given in Fig.4.25. a), while the VTC $v_O(v_I)$ is in Fig.4.25. b).

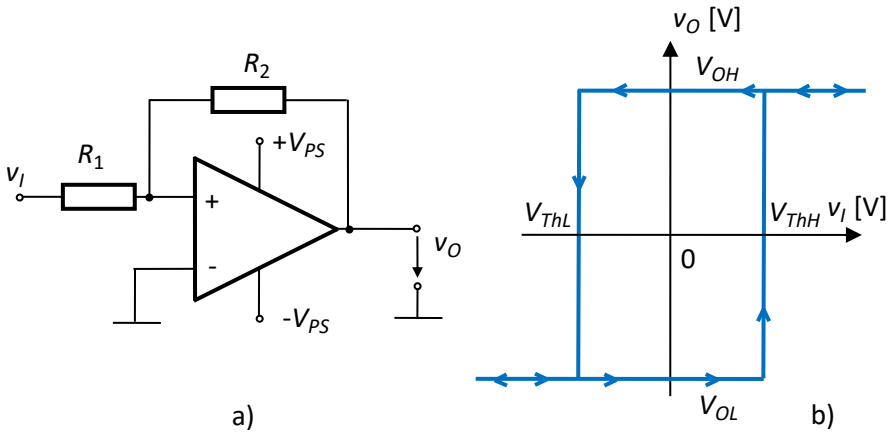


Fig.4.25. Noninverting hysteresis comparator with symmetric thresholds
a) circuit; b) VTC $v_O(v_I)$.

To determine the threshold voltages, the same condition as for simple comparators is used: the threshold(s) is the value of the input voltage, when the differential voltage is zero.

$$V_{Th} = v_I \mid_{v_D = 0}$$

$$v_D = v^+ - v^-$$
$$v^+ = \frac{R_1}{R_1 + R_2} \cdot v_O + \frac{R_2}{R_1 + R_2} \cdot v_I$$
$$v^- = 0\ \text{V}$$

$$v^+ = v^- \Rightarrow \frac{R_1}{R_1 + R_2} \cdot v_O + \frac{R_2}{R_1 + R_2} \cdot V_{Th} = 0$$
$$V_{Th} = -\frac{R_1}{R_2} \cdot v_O$$

The high threshold voltage V_{ThH} is obtained for the low output V_{OL}, as a consequence of the minus sign in the expression of V_{Th}. The values of the two threshold voltages are:

$$V_{ThH} = -\frac{R_1}{R_2} \cdot V_{OL}$$
$$V_{ThL} = -\frac{R_1}{R_2} \cdot V_{OH}$$

When the input voltage increases, the active threshold is V_{ThH}, that is the output voltage switches from V_{OL} to V_{OH} when the input voltage crosses $V_{ThH.}$ When the input voltage decreases, the active threshold is V_{ThL}, that is the output voltage switches from V_{OH} to V_{OL} when the input voltage crosses V_{ThL}. The memory of lag feature is, once again, obvious. The arrows on the VTC $v_O(v_I)$ (Fig.4.24. b)) show the active threshold, based on the ascending/descending trend of the input voltage. Sample waveforms for $v_I(t)$ and $v_O(t)$ are shown in Fig.4.26.

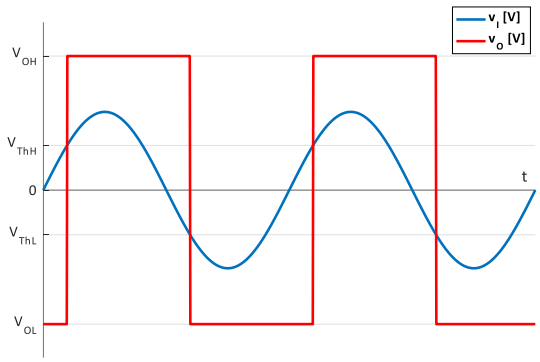


Fig.4.26. Waveforms for $v_I(t)$ and $v_O(t)$ for the noninverting hysteresis comparator with symmetric thresholds

The hysteresis is centred on 0 V (symmetric thresholds). The width of the hysteresis depends on R_1, R_2, V_{OH} and V_{OL}. Changing any of these four values leads to a change in the width of the hysteresis.

$$\Delta V_{Th} = V_{ThH} - V_{ThL} = \frac{R_1}{R_2} \cdot (V_{OH} - V_{OL})$$

Hysteresis comparators with asymmetric thresholds

Both the inverting and the noninverting hysteresis comparator can be modified so that the threshold voltages are no longer symmetric with respect to 0 V. The idea is to add an additional dc voltage source, V_{Ref}, on the other input of the op-amp (one input already receives v_I).

An inverting hysteresis comparator with asymmetric thresholds is shown in Fig.4.27. a), and the corresponding VTC $v_O(v_I)$ is in Fig.4.27. b).

$$v_D = v^+ - v^-$$

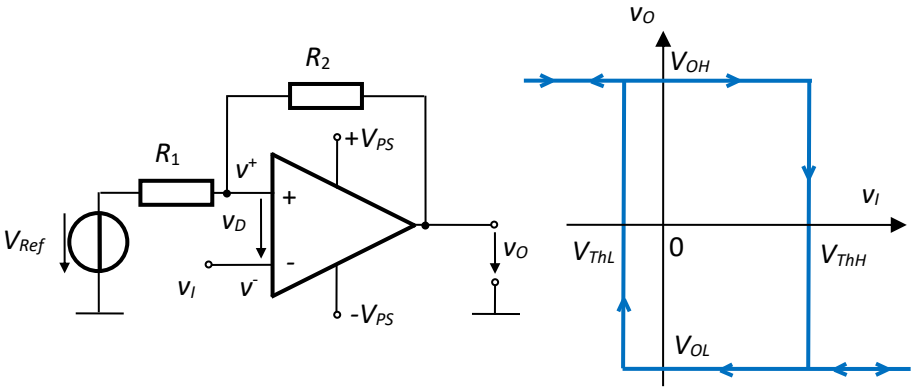
$$v^+ = \frac{R_1}{R_1+R_2}\cdot v_O + \frac{R_2}{R_1+R_2}\cdot V_{Ref}$$

$$v^- = v_I$$

$$v^+ = v^- \Rightarrow \frac{R_1}{R_1+R_2}\cdot v_O + \frac{R_2}{R_1+R_2}\cdot V_{Ref} = V_{Th}$$

$$V_{ThH} = \frac{R_1}{R_1+R_2}\cdot V_{OH} + \frac{R_2}{R_1+R_2}\cdot V_{Ref}$$

$$V_{ThL} = \frac{R_1}{R_1+R_2}\cdot V_{OL} + \frac{R_2}{R_1+R_2}\cdot V_{Ref}$$



a) b)

Fig.4.27. Inverting hysteresis comparator with asymmetric thresholds
a) circuit; b) VTC $v_O(v_I)$.

When V_{Ref} = 0 V, the thresholds become symmetric with respect to 0 V. Both thresholds move to the right on the horizontal axis for V_{Ref} > 0 V, or to the left, for V_{Ref} < 0 V. The width of the hysteresis is not influenced by the change of V_{Ref}.

A noninverting hysteresis comparator with asymmetric thresholds is presented in Fig.4.28. a), along with its VTC $v_O(v_I)$ in Fig.4.28. b). The dc voltage V_{Ref} can be obtained by using a resistive divider, connected between one of the supply terminals and the inverting input, as shown in Fig.4.28. a), or from a potentiometer, if an adjustable V_{Ref} is needed.

$$v_D = v^+ - v^-$$

$$v^+ = \frac{R_1}{R_1+R_2}\cdot v_O + \frac{R_2}{R_1+R_2}\cdot v_I$$

$$v^- = V_{Ref} = \frac{R_3}{R_3+R_4}\cdot(-V_{PS})$$

$$v^+ = v^- \Rightarrow \frac{R_1}{R_1+R_2}\cdot v_O + \frac{R_2}{R_1+R_2}\cdot V_{Th} = V_{Ref}$$

$$V_{Th} = \left(1+\frac{R_1}{R_2}\right)\cdot V_{Ref} - \frac{R_1}{R_2}\cdot v_O$$

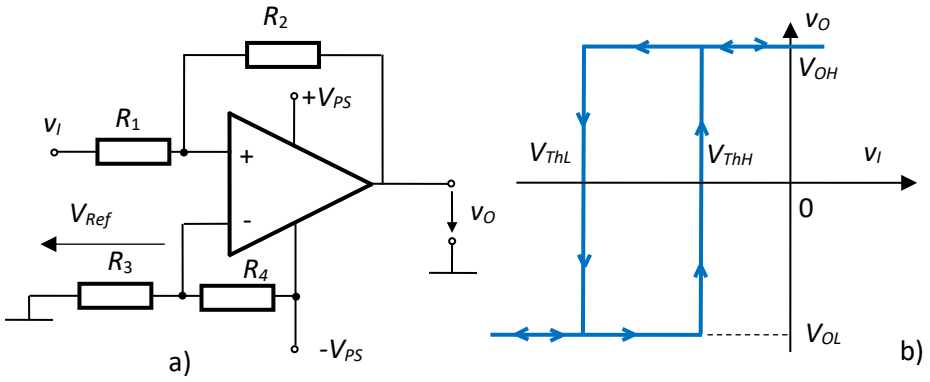


Fig.4.28. Noninverting hysteresis comparator with asymmetric thresholds
a) circuit; b) VTC $v_O(v_I)$.

$$V_{ThH} = (1 + \frac{R_1}{R_2}) \cdot V_{Ref} - \frac{R_1}{R_2} \cdot V_{OL}$$

$$V_{ThH} = (1 + \frac{R_1}{R_2}) \cdot \frac{R_3}{R_3 + R_4} \cdot (-V_{PS}) - \frac{R_1}{R_2} \cdot V_{OL}$$

$$V_{ThL} = (1 + \frac{R_1}{R_2}) \cdot V_{Ref} - \frac{R_1}{R_2} \cdot V_{OH}$$

$$V_{ThL} = (1 + \frac{R_1}{R_2}) \cdot \frac{R_3}{R_3 + R_4} \cdot (-V_{PS}) - \frac{R_1}{R_2} \cdot V_{OH}$$

Because $V_{Ref} < 0$, the two threshold voltages V_{ThL} and V_{ThH} are shifted towards the left (towards negative values) on the horizontal axis.

Examples

1. Design and size an inverting hysteresis comparator with $V_{ThH} = 3V$ and $V_{ThL} = -3V$, with a differential supply of ±12V. Plot the VTC $v_O(v_I)$. Plot $v_I(t)$ and $v_O(t)$ for:
i) $v_I(t) = 2\sin\omega t$ [V][Hz]
ii) $v_I(t) = 8\sin\omega t$ [V][Hz].

Solution:
The circuit that meets the requirements is the one in Fig.4.23, inverting hysteresis comparator with symmetric thresholds.

$$V_{ThH} = \frac{R_1}{R_1 + R_2} \cdot V_{OH} \Rightarrow \frac{R_1}{R_1 + R_2} = \frac{V_{ThH}}{V_{OH}} = \frac{1}{4}$$

$$V_{ThL} = \frac{R_1}{R_1 + R_2} \cdot V_{OL} \Rightarrow \frac{R_1}{R_1 + R_2} = \frac{V_{ThL}}{V_{OL}} = \frac{1}{4}$$

$$R_1 + R_2 = 4 \cdot R_1 \Rightarrow R_2 = 3 \cdot R_1$$

Any two resistors that meet the condition can be chosen. Some possible values are:

$R_1 = 2$ kΩ; $R_2 = 6$ kΩ
$R_1 = 5$ kΩ; $R_2 = 15$ kΩ
$R_1 = 3.2$ kΩ; $R_2 = 9.6$ kΩ

The VTC $v_O(v_I)$ is shown in Fig.4.29, and the waveforms for $v_I(t)$ and $v_O(t)$ are in Fig.4.30.

For $v_I(t)$ = 2sinωt [V][Hz], the input voltage never crosses any of the two thresholds, meaning that the output voltage never switches. The output voltage is constant, at the value of either V_{OH} or V_{OL}.

For $v_I(t)$ = 8sinωt [V][Hz], the input voltage crosses both thresholds, the active threshold is given by the trend of the input voltage (increasing/decreasing) - Fig.4.30. b).

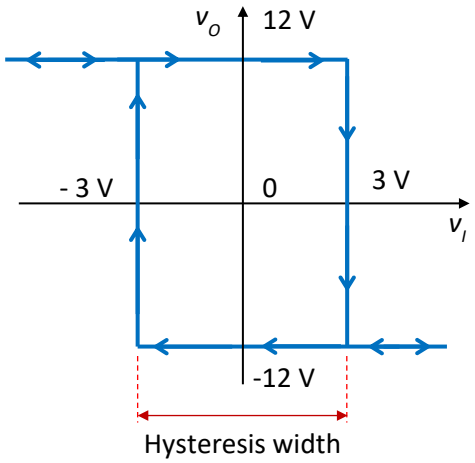


Fig.4.29. VTC $v_O(v_I)$

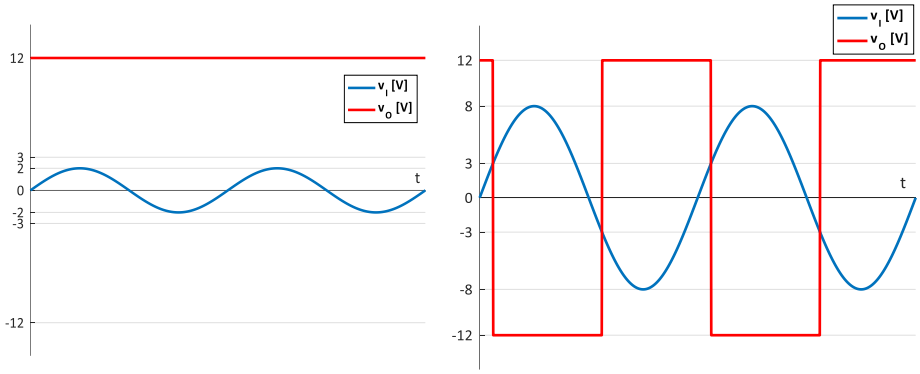


Fig.4.30. Waveforms of $v_I(t)$ and $v_O(t)$
a) case i); b) case ii).

2. Modify the circuit in **Example 1**, so that the width of the hysteresis is halved.

Solution:
The width of the hysteresis in **Example 1** is:

$$\Delta V_{Th} = V_{ThH} - V_{ThL} = \frac{R_1}{R_1 + R_2} \cdot (V_{OH} - V_{OL})$$

$$\Delta V_{Th} = 3 - (-3) = 6 \text{ V}$$

The new width is:

$$\Delta V_{Th,new} = \Delta V_{Th} / 2$$

$$\frac{R_{1new}}{R_{1new} + R_{2new}} \cdot (V_{OH} - V_{OL}) = 3 \text{ V}$$

The supply voltages are commonly left unchanged, so, to modify the width of the hysteresis, the resistors are subject to change.

$$\frac{R_{1new}}{R_{1new}+R_{2new}} \cdot (12 - (-12)) = 3$$
$$\frac{R_{1new}}{R_{1new}+R_{2new}} \cdot 24 = 3$$
$$\frac{R_{1new}}{R_{1new}+R_{2new}} = \frac{1}{8}$$
$$R_{1new} + R_{2new} = 8 \cdot R_{1new} \Rightarrow \quad R_{2new} = 7 \cdot R_{1new}$$

Any values for R_{1new} and R_{2new} that meet the condition can be chosen. Also, it is not mandatory to change both resistors, one of them can be kept at the previous value.
Possible solutions are:

$$R_{1new} = 2\ \text{k}\Omega;\ R_{2new} = 14\ \text{k}\Omega$$
$$R_{1new} = 3\ \text{k}\Omega;\ R_{2new} = 21\ \text{k}\Omega.$$

3. Modify the circuit in **Example 1**, so that the hysteresis is shifted towards the right with 2 V. Plot $v_I(t)$and $v_O(t)$ for $v_I(t) = 8\sin\omega t$ [V][Hz].

Solution:
The circuit in Fig.4.23 is modified by adding a dc voltage V_{Ref} at the noninverting input of the op-amp, as shown in Fig.4.27. a). The threshold voltages are computed as:

$$V_{ThH} = \frac{R_1}{R_1+R_2} \cdot V_{OH} + \frac{R_2}{R_1+R_2} \cdot V_{Ref}$$
$$V_{ThL} = \frac{R_1}{R_1+R_2} \cdot V_{OL} + \frac{R_2}{R_1+R_2} \cdot V_{Ref}$$

From the expressions of the threshold voltages, the 2 V shift towards the right is given by:

$$\frac{R_2}{R_1+R_2} \cdot V_{Ref} = 2\ \text{V}$$
$$V_{Ref} = \frac{R_2}{R_1+R_2} \cdot 2 = 2 \cdot (1 + \frac{R_1}{R_2})$$

A pair of values for the resistors is:

$$R_1 = 2\ \text{k}\Omega;\ R_2 = 6\ \text{k}\Omega$$

which results in

$$V_{Ref} = 2 \cdot (1 + \frac{2}{6})$$
$$V_{Ref} = 2.67\ \text{V}$$

The new values of the threshold voltages are obtained by adding 2 V to the previous ones. The width of the hysteresis remains unchanged.

$$V_{ThH} = \frac{R_1}{R_1+R_2} \cdot V_{OH} + \frac{R_2}{R_1+R_2} \cdot V_{Ref}$$
$$V_{ThH} = 3\ \text{V} + 2\ \text{V} = 5\ \text{V}$$
$$V_{ThL} = -3\ \text{V} + 2\ \text{V} = -1\ \text{V}$$
$$\Delta V_{Th} = 5\ \text{V} - (-1)\ \text{V} = 6\ \text{V}$$

The waveforms of $v_I(t)$ and $v_O(t)$ are shown in Fig.4.31.

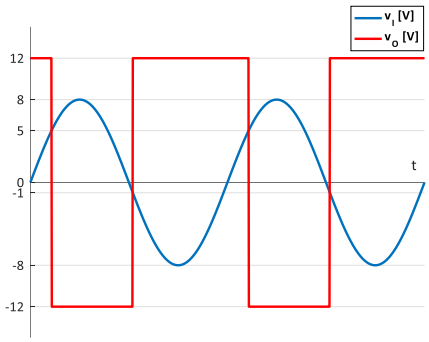


Fig.4.31. Waveforms of $v_I(t)$ and $v_O(t)$

4. Plot the VTC $v_O(v_I)$ for the circuit in Fig.4.28. a), if R_1 = 2 kΩ, R_2 = 10 kΩ, R_3 = 3 kΩ, R_4 = 6 kΩ, $\pm V_{PS}$ = ±12 V. Plot $v_I(t)$ and $v_O(t)$ when:
i) $v_I(t) = 2\sin\omega t$ [V][Hz]
ii) $v_I(t) = 8\sin\omega t$ [V][Hz].

Solution:
The circuit in Fig.4.28. a) is a noninverting hysteresis comparator, with asymmetric thresholds. To plot the VTC $v_O(v_I)$, the values of the threshold voltages, as well as $V_{Ref,}$ are computed:

$$v^- = V_{Ref} = \frac{R_3}{R_3 + R_4} \cdot (-V_{PS})$$

$$V_{Ref} = \frac{3}{9} \cdot (-12)\ \text{V} = -4\ \text{V}$$

$$V_{ThH} = \left(1 + \frac{R_1}{R_2}\right) \cdot V_{Ref} - \frac{R_1}{R_2} \cdot V_{OL}$$

$$V_{ThL} = \left(1 + \frac{R_1}{R_2}\right) \cdot V_{Ref} - \frac{R_1}{R_2} \cdot V_{OH}$$

$$V_{ThH} = \left(1 + \frac{2}{10}\right) \cdot (-4) - \frac{2}{10} \cdot (-12) = -4.8 + 2.4 = -2.4\ [\text{V}]$$

$$V_{ThL} = \left(1 + \frac{2}{10}\right) \cdot (-4) - \frac{2}{10} \cdot (12) = -4.8 - 2.4 = -7.2\ [\text{V}]$$

The VTC $v_O(v_I)$ is shown in Fig.4.32.

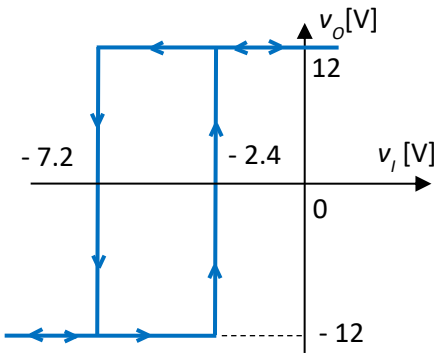
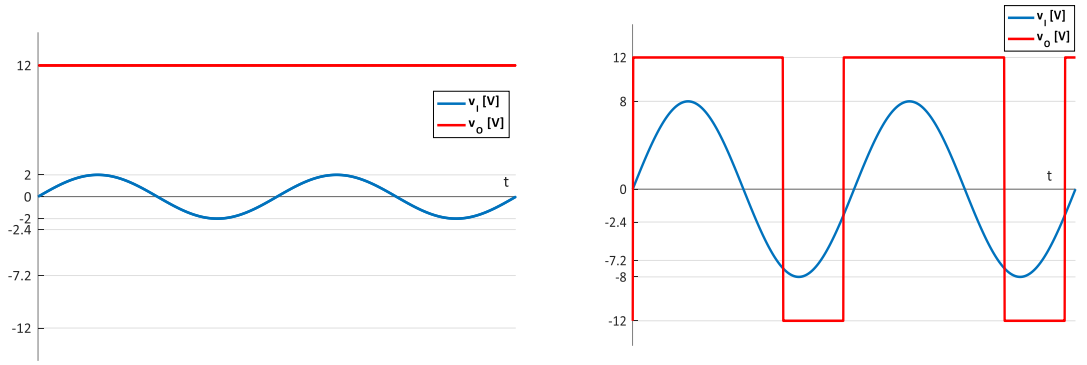


Fig.4.32. VTC $v_O(v_I)$

When the input voltage is increasing (left to right on the horizontal axis), the active threshold is V_{ThH}; when the input voltage is decreasing, the active threshold is V_{ThL}. The waveforms for $v_I(t)$ and $v_O(t)$, for both cases, are depicted in Fig.4.33.



a) b)

Fig.4.33. Waveforms of $v_I(t)$ and $v_O(t)$
a) case i); b) case ii).

Problems

1. Design and size an inverting hysteresis comparator with symmetric thresholds, V_{ThH} = 5 V and V_{ThL} = -5 V, differential supply of ±15 V. Plot the VTC $v_O(v_I)$, then plot $v_I(t)$ and $v_O(t)$ assuming $v_I(t) = 12\sin\omega t$ [V][Hz].

2. Modify the circuit in **Problem 1**, so that the width of the hysteresis is 5 V.

3. Add a dc voltage source V_{Ref} = 6 V to the circuit in in **Problem 1**. Draw the new circuit. Plot the VTC $v_O(v_I)$. Plot $v_I(t)$ and $v_O(t)$ for $v_I(t) = 12\sin\omega t$ [V][Hz]. Compute the width of the hysteresis.

4. Add a dc voltage source V_{Ref} = -6 V to the circuit in in **Problem 1**. Draw the new circuit. Plot the VTC $v_O(v_I)$. Plot $v_I(t)$ and $v_O(t)$ for $v_I(t) = 12\sin\omega t$ [V][Hz]. Compute the width of the hysteresis.

5. Plot the VTC $v_O(v_I)$ for the circuit in Fig.4.25 a), if R_1 = 4 kΩ, R_2 = 6 kΩ, $\pm V_{PS}$ = ±12 V. Compute the width of the hysteresis. Plot $v_I(t)$ and $v_O(t)$ for:
i) $v_I(t) = 2\sin\omega t$ [V][Hz]
ii) $v_I(t) = 10\sin\omega t$ [V][Hz].

6. Plot the VTC $v_O(v_I)$ for the circuit in Fig.4.28 a), if R_1 = 1 kΩ, R_2 = 4 kΩ, V_{Ref} = 2 V, $\pm V_{PS}$ = ±12 V. Plot $v_I(t)$ and $v_O(t)$ for:
i) $v_I(t) = 2\sin\omega t$ [V][Hz]
ii) $v_I(t) = 8\sin\omega t$ [V][Hz].
Modify the circuit so that V_{Ref} is obtained from V_{PS}. Size the newly added components.

7. Plot the VTC $v_O(v_I)$ for the circuit in Fig.4.28 a), if R_1 = 1 kΩ, R_2 = 4 kΩ, V_{Ref} = -2 V, $\pm V_{PS}$ = ±20 V. Plot $v_I(t)$ and $v_O(t)$ for:
i) $v_I(t) = 2\sin\omega t$ [V][Hz]
ii) $v_I(t) = 8\sin\omega t$ [V][Hz].
Modify the circuit so that V_{Ref} is obtained from $-V_{PS}$. Size the newly added components.

8. Modify the circuit in **Problem 7**, so that the width of the hysteresis is halved. Draw the new circuit and plot the VTC $v_O(v_I)$.

For all the comparators discussed in this chapter, the threshold voltages depend on the extreme values of the output voltage, which in turn are given by the values of the supply voltages. To eliminate the dependence of the output voltages on the power supplies, a resistor and two Zener diodes are connected at the output of the op-amp, as shown in Fig.4.34.

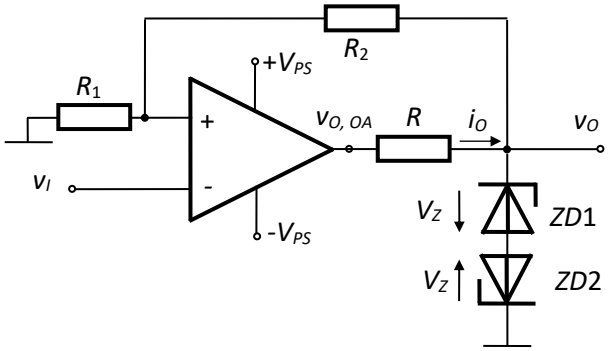


Fig.4.34. Inverting hysteresis comparator with output voltage independent of the two power supplies

Usually, the two Zener diodes are identical, so that the extreme values of the output voltage are equal, in absolute value. Resistor *R* ensures an appropriate value of the current through the two Zener diodes:

$$i_O = \frac{v_{O,\,OA} - v_O}{R}$$

When the differential voltage $v_D > 0$ V, the voltage at the output of the op-amp is $v_{O,\,OA} = V_{OH} = +V_{PS}$. Thus, *ZD*1 is in breakdown, and *ZD*2 is *on*, in forward bias. The extreme value of the output voltage is:

$$V_{OH} = V_Z + v_{ZD,\,on} = V_Z + 0.7 \text{ [V]}$$

When the differential voltage $v_D < 0$ V, the voltage at the output of the op-amp is $v_{O,\,OA} = V_{OL} = -V_{PS}$. Thus, *ZD*2 is in breakdown, and *ZD*1 is *on*, in forward bias. The extreme value of the output voltage is:

$$V_{OL} = -(V_Z + v_{ZD,\,on}) = -(V_Z + 0.7) \text{ [V]}$$

4.2.4 Applications of hysteresis comparators

Hysteresis comparators are used to ensure the immunity of comparators to the noise that occurs in signal processing circuits. The difference between the two threshold voltages (the width of the hysteresis) is small, between 100 and 200 mV, but enough to eliminate the effect of noise.

Hysteresis comparators are used in digital circuits (logic inverters, monostable and bistable circuits), due to their memory property.

Hysteresis comparators are also found in analog-to-digital converters, where they transform the triangular or sinusoidal input signal into a rectangular (digital) signal.

Another important application of hysteresis comparators is oscillators. For the circuit shown in Fig.4.35. a), an *RC* network is connected on the negative feedback loop of an op-amp, which also has positive feedback. The circuit does not have an input voltage, hence it is an oscillator – produces an output signal, rectangular in this case. The signal obtained at the inverting input (charging and discharging of the capacitor) can be considered triangular, so the circuit is called rectangular and triangular signal generator. Sample waveforms are shown in Fig. 4.35. b).

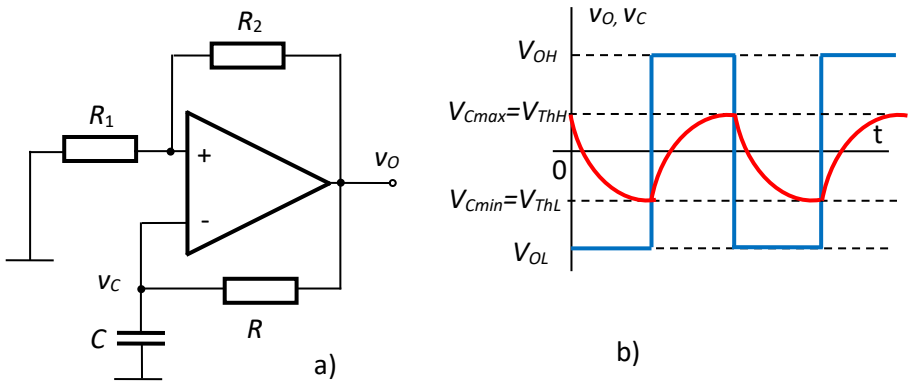


Fig.4.35. RC and positive feedback op-amp oscillator
a) circuit; b) waveforms of $v_C(t)$ and $v_O(t)$.

4.3 Voltage amplifiers with op-amp

The operational amplifier can be modelled as a voltage-controlled voltage source (*VCVS*), as previously shown. The output voltage is computed as:

$$v_O = a \cdot v_D$$
$$v_D = v^+ - v^-$$

The parameters of the op-amp are very close to the parameters of an ideal electronic amplifier, with the extremely high gain, considered to be infinite:

$$v_O = \infty \cdot v_D$$

To obtain an output voltage that is different from the extreme values V_{OL} or V_{OH}, the differential voltage v_D must be kept at 0 V, always. This is achieved by connecting an external circuit between the output of the op-amp and the inverting input, that is building a *negative feedback loop* (NF). Thus, the output voltage is now an indeterminate form, meaning the output voltage can now be any value between V_{OL} or V_{OH}:

$$v_D = 0,\ v_O = \infty \cdot 0 = \text{constant}$$
$$v_O \in [V_{OL}; V_{OH}]$$

A qualitative analysis that explains how the differential voltage v_D is kept at 0 V, by means of the negative feedback, is performed on the circuit in Fig.4.36, a noninverting voltage amplifier with op-amp (the input voltage is connected to the noninverting input).

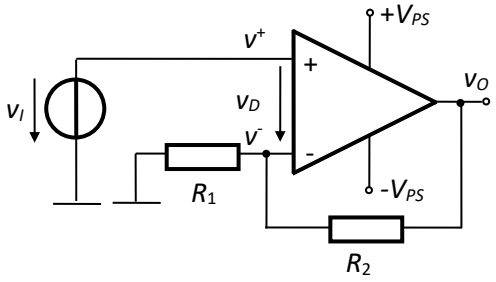


Fig.4.36. Noninverting voltage amplifier with op-amp

The circuit's equations are:

$$v^+ = v_I$$
$$v^- = \frac{R_1}{R_1 + R_2} \cdot v_O$$
$$v_D = v_I - \frac{R_1}{R_1 + R_2} \cdot v_O$$

There are two possible situations to be analysed: when v_I increases and when v_I decreases.

$$v_I \uparrow;\ v^+ \uparrow;\ v_D \uparrow;\ v_O \uparrow;\ v^- \uparrow;\ v_D \downarrow$$
$$v_I \downarrow;\ v^+ \downarrow;\ v_D \downarrow;\ v_O \downarrow;\ v^- \downarrow;\ v_D \uparrow$$

In both cases, the negative feedback counteracts the effect of the input voltage upon v_D: if v_D tries to increase, the op-amp and the negative feedback loop will bring v_D back down; when v_D tries to decrease, the op-amp and the negative feedback loop will bring v_D back up. This was, v_D is kept at 0 V. The same analysis can be performed for an inverting amplifier (the input voltage is connected to the inverting input).

Based on where the input voltage is connected, amplifiers with op-amp can be inverting, noninverting, summing (inverting or noninverting), differential (Table 4.3). Summing amplifiers have two or more input voltages, connected at the same input of the op-amp. Differential amplifiers have two input voltages, each connected to one input of the op-amp.

Table 4.3. Types of voltage amplifiers

Noninverting input v^+	**Inverting input v^-**	**Type of amplifier**
v_I	0 V	noninverting amplifier
0 V	v_I	inverting amplifier
v_{I1}, v_{I2} ... v_{In}	0 V	summing noninverting amplifier
0 V	v_{I1}, v_{I2} ... v_{In}	summing inverting amplifier
v_{I1}	v_{I2}	differential amplifier

4.3.1 Noninverting amplifier

The noninverting amplifier with op-amp is shown in Fig.4.37.

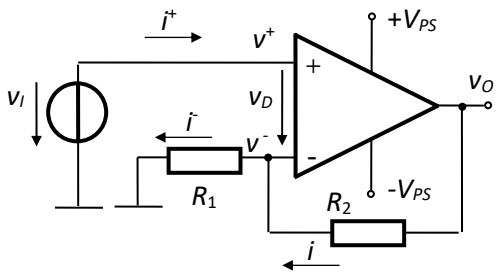


Fig.4.37. Noninverting amplifier

Through the negative feedback loop, the differential voltage v_D is maintained at 0 V. An op-amp without feedback (open loop) behaves as an ideal amplifier, with the open loop gain $a \to \infty$. By adding the negative feedback loop, the gain of the circuit decreases to a finite value.

Voltage gain and active region

The starting point in analysing the circuit's behaviour and determining the voltage gain is that the differential voltage is always null, as a consequence of the negative feedback. The circuit's equations are:

$$v_D = 0\ \text{V} \Rightarrow v^+ = v^-$$

$$v^+ = v_I$$

$$v^- = \frac{R_1}{R_1 + R_2} \cdot v_O$$

$$v_I = \frac{R_1}{R_1 + R_2} \cdot v_O$$

$$A_v = \frac{v_O}{v_I} = \frac{R_1 + R_2}{R_1} = 1 + \frac{R_2}{R_1} = 1 + \frac{R_{NF}}{R_-}$$

The voltage gain is the ratio between the output and the input voltages, and has a finite value given by the resistors that were added outside the op-amp, to build the negative feedback loop.

The gain can also be computed by using the current that flows through the resistors, R_1 and R_2 are in series (no current consumption on the inputs of the op-amp).

$$i = \frac{v^-}{R_1} = \frac{v_O - v^-}{R_2}$$

$$v^+ = v^- = v_I \Rightarrow \frac{v_I}{R_1} = \frac{v_O - v_I}{R_2}$$

$$A_v = \frac{v_O}{v_I} = \frac{R_1 + R_2}{R_1} = 1 + \frac{R_2}{R_1} = 1 + \frac{R_{NF}}{R_-}$$

The extreme values of the output voltage are still V_{OH} and V_{OL}, and the range of values of the input voltage for which the circuit works as an amplifier is:

$$v_O \in [V_{OL}; V_{OH}] \Rightarrow v_I \in \left[\frac{V_{OL}}{A_v}; \frac{V_{OH}}{A_v}\right]$$

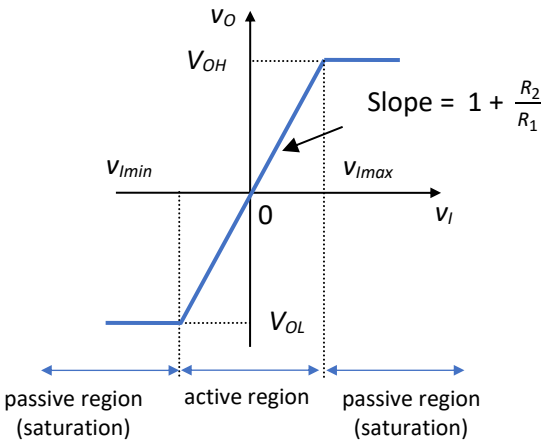


Fig.4.38. VTC $v_O(v_I)$ for the noninverting amplifier

The range of values of the input voltage for which the circuit works as an amplifier is called the *active region* of the amplifier. The active region becomes narrower when the voltage gain increases.

The VTC $v_O(v_I)$ is a line located in the 1st and 3rd quadrants, that passes through the origin (the output is zero for zero input) - Fig.4.38. The slope of the line is the voltage gain of the amplifier. When the input exceeds the active region, the output voltage is clipped/limited to the V_{OH} and V_{OL}, and the amplifier works in the *passive region*.

Input and output resistances

When the amplifier is connected in a circuit, voltage dividers appear both at the input (between the output resistance of the previous stage and the input resistance of the amplifier) and at the output (between the output resistance of the amplifier and the input resistance of the next stage). These voltage dividers influence (decrease) the gain of the entire circuit.

The input resistance is the equivalent resistance seen by the input source, measured between the terminal it is connected to, and ground.

$$R_i = \frac{v_i}{i_I} = \frac{v^+}{i^+} = \frac{v^+}{0} = \infty$$

In a similar way, the output resistance is the equivalent resistance seen from the output towards the input, when the input is grounded. To compute the output resistance, Ohm's law is once again used, with the open-circuit output voltage and the short-circuit current, assuming $R_L = 0\ \Omega$. The short-circuit current is $i_{Osc} = \infty$.

$$R_o = \frac{v_{Oopen}}{i_{Osc}} = \frac{v_{Oopen}}{\infty} = 0\ \Omega$$

The noninverting amplifier is ideal, from the point of view of input and output resistances, $R_i = \infty$ and $R_o = 0\ \Omega$. The model of a noninverting amplifier with op-amp as a voltage-controlled voltage source, including R_i and R_o, is shown in Fig.4.39.

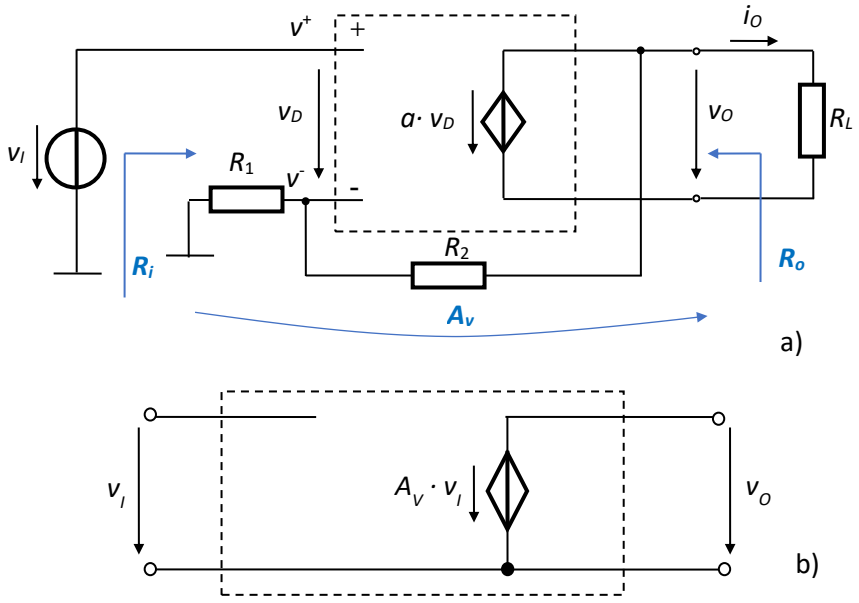


Fig.4.39. Modelling the noninverting amplifier as a VCVS
a) with the model of the op-amp; b) without the model of the op-amp.

By changing either or both resistors on the negative feedback loop, the gain of the amplifier is changed.

When $A_v = 1$ (unity gain), the amplifier is called noninverting voltage follower. A unity gain can be obtained either by setting R_1 to infinity (open circuit) or R_2 to 0 Ω (shortcircuit). When both resistors are changed to these values at the same time (recommended), it is said that the circuit has total negative feedback (Fig.4.40).

$$v_D = 0\ \text{V} \Rightarrow v^+ = v^-$$
$$v^+ = v_I$$
$$v^- = v_O$$

$$v_I = v_O$$
$$A_v = \frac{v_O}{v_I} = 1$$

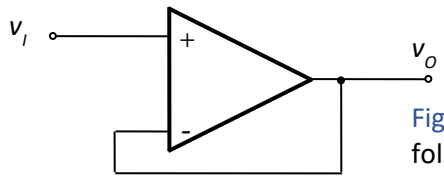


Fig.4.40. Noninverting voltage follower

An adjustable voltage gain is obtained by connecting a potentiometer in series with either R_1 or R_2, or in between the two resistors, as shown in Fig.4.41.

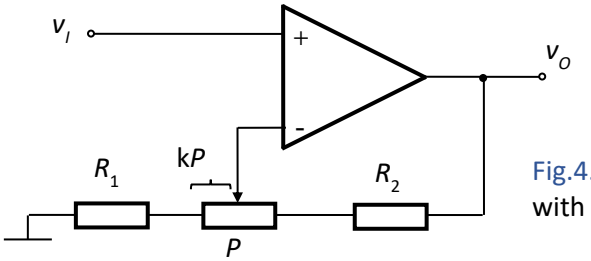


Fig.4.41. Noninverting amplifier with adjustable gain

The circuit's equations:

$$v_D = 0\ \text{V} \Rightarrow v^+ = v^-$$
$$v^+ = v_I$$
$$v^- = \frac{R_1 + \text{k}P}{R_1 + R_2 + P} \cdot v_O$$
$$v_I = \frac{R_1 + \text{k}P}{R_1 + R_2 + P} \cdot v_O$$
$$A_v = \frac{v_O}{v_I} = \frac{R_1 + R_2 + P}{R_1 + \text{k}P}$$
$$A_{vmax} = \frac{R_1 + R_2 + P}{R_1} = 1 + \frac{R_2 + P}{R_1}$$
$$A_{vmin} = \frac{R_1 + R_2 + P}{R_1 + P} = 1 + \frac{R_2}{R_1 + P}$$

$$A_v \in [A_{vmin}; A_{vmax}]$$

The maximum gain is obtained for k = 0, when the tap of the potentiometer is at the extreme left, whereas the minimum gain is obtained for k = 1, extreme right position for the tap of the potentiometer.

Amplifiers with op-amp are usually directly coupled (the variable input signal is directly connected to one of the op-amp's inputs). When the input signal has both a variable component and a dc component, capacitive coupling is used. A *coupling capacitor* is connected between the input signal and the input of the op-amp, as shown in Fig.4.42. The coupling capacitor C_i and resistor R must be chosen so that the gain decreases at low frequencies and is zero for dc components. Resistor R ensures a charging path for capacitor C_i in transient regime.

Capacitive coupling is also needed when the op-amp has unipolar supply (see Section 4.5.2).

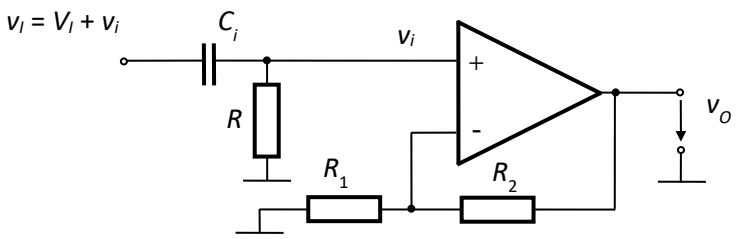


Fig.4.42. Noninverting amplifier with capacitive coupling

4.3.2 Inverting amplifier

For an inverting amplifier with op-amp, the input voltage is connected to the inverting input - Fig.4.43.

To determine the gain, the starting point is the same as for the noninverting amplifier: $v_D = 0$ V, due to the negative feedback.

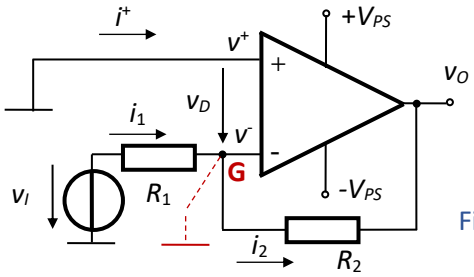


Fig.4.43. Inverting amplifier

$$v_D = 0 \text{ V} \Rightarrow v^+ = v^-$$

$$v^+ = 0 \text{ V}$$

$$v^- = \frac{R_1}{R_1 + R_2} \cdot v_O + \frac{R_2}{R_1 + R_2} \cdot v_I$$

$$v^- = 0 \text{ V}$$

$$\frac{R_1}{R_1 + R_2} \cdot v_O + \frac{R_2}{R_1 + R_2} \cdot v_I = 0 \text{ V}$$

$$\frac{R_1}{R_1 + R_2} \cdot v_O = -\frac{R_2}{R_1 + R_2} \cdot v_I$$

$$A_v = \frac{v_O}{v_I} = -\frac{R_2}{R_1} = -\frac{R_{NF}}{R_-}$$

The gain is determined by the same ratio of resistors as for the noninverting amplifier. The gain is negative, meaning there will be a 180° phase shift between the input and output signals (when v_I is positive, v_O is negative, and vice versa).

Because of the negative feedback, v^- is also 0 V, even if the inverting input is not actually connected to ground. Point G is hence called *virtual ground* (the dotted line represents a virtual connection to ground).

Another method for determining the gain is by using the currents through R_1 and R_2 (same current through both resistors, no current consumption on the inputs of the op-amp).

$$i_1 = \frac{v_I - v^-}{R_1} = \frac{v_I}{R_1}$$

$$i_2 = \frac{v^- - v_O}{R_2} = -\frac{v_O}{R_2}$$

$$i_1 = i_2 \Rightarrow \frac{v_I}{R_1} = -\frac{v_O}{R_2}$$
$$A_v = \frac{v_O}{v_I} = -\frac{R_2}{R_1} = -\frac{R_{NF}}{R_-}$$

The extreme values of the output voltage are still V_{OH} and V_{OL}, and the active region is:

$$v_O \in [V_{OL}; V_{OH}] \Rightarrow v_I \in [\frac{V_{OH}}{A_v}; \frac{V_{OL}}{A_v}]$$

The minimum value of the input voltage for which the circuit works as an amplifier is computed using V_{OH}, and the maximum value is computed using V_{OL}, since the gain is negative.

The VTC $v_O(v_I)$ is a line located in the 2nd and 4th quadrants, that passes through the origin (the output is zero for zero input) - Fig.4.44. The slope of the line is the voltage gain of the amplifier. When the input exceeds the active region, the output voltage is clipped/limited to the V_{OH} and V_{OL}, and the amplifier works in the *passive region*.

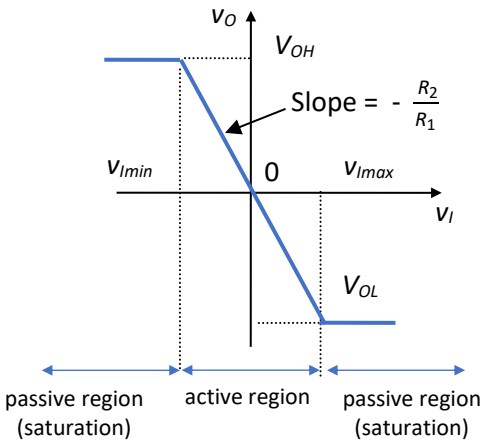


Fig.4.38. VTC $v_O(v_I)$ for the inverting amplifier

Input and output resistances

The resistance seen by the input source v_I towards ground is R_1 (G is virtual ground), smaller than the one of the noninverting amplifier. The output resistance is 0 Ω, same as for the noninverting amplifier.

$$R_i = R_1$$
$$R_o = 0\ \Omega$$

Modelling the inverting amplifier as a voltage-controlled voltage source, with the values of R_i and R_o, is shown in Fig.4.45.

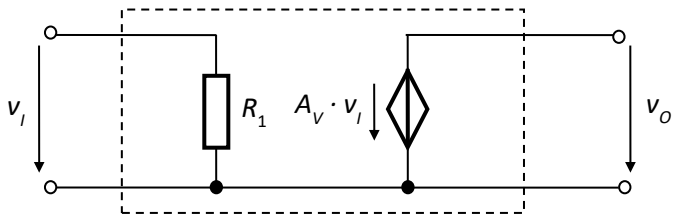


Fig.4.45. Modelling the inverting amplifier as a VCVS

There are ways of obtaining a high R_i and a high gain. For a high input resistance, R_1 must be very high – tens, hundreds of kΩ or even more. To obtain a high gain (in absolute value), R_2 must be even

bigger than R_1 (hundreds, thousands of kΩ). Such high values for resistors are uncommon for op-amp circuits.

A solution that provides a high gain and high input resistance using common values for R_1 and R_2 is shown in Fig.4.46. Resistor R_2 from the circuit in Fig.4.43 is replaced by a T-shaped resistor network.

Resistors R_{21} and R_3 are in parallel, connected between points N and ground (point G is virtual ground), meaning they share the same voltage drop.

$$R_{21} \cdot i_2 = R_3 \cdot i_3$$

Point N is a current node:

$$i_{22} = i_2 + i_3$$

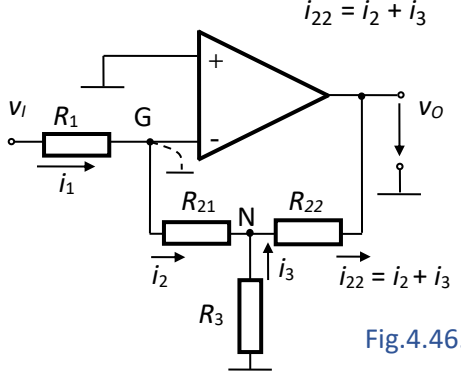


Fig.4.46. T-network inverting amplifier

The voltage drop across resistors R_{21} and R_{22} is:

$$-v_O = R_{21} \cdot i_2 + R_{22} \cdot (i_2 + i_3)$$

$$v_O = -(R_{21} \cdot i_2 + R_{22} \cdot i_2 + R_{22} \cdot \frac{R_{21}}{R_3} \cdot i_2)$$

$$v_O = -(R_{21} + R_{22} + \frac{R_{22} \cdot R_{21}}{R_3}) \cdot i_2$$

To determine the gain, a relationship that contains v_O and v_I must be found:

$$i_2 = i_1 = \frac{v_I}{R_1}$$

$$v_O = -(R_{21} + R_{22} + \frac{R_{22} \cdot R_{21}}{R_3}) \cdot \frac{v_I}{R_1}$$

$$A_V = -(\frac{R_{21} + R_{22}}{R_1} + \frac{R_{22} \cdot R_{21}}{R_1 \cdot R_3})$$

The gain is inversely proportional with R_1 and R_3. Since the input resistance is given by R_1, the values for R_1 cannot be small. So, to obtain a high gain, R_3 must be chosen as small as possible.

Example

Compute the gain for the circuit in Fig.4.46, if: $R_1 = 5$ kΩ, $R_{21} = 3$ kΩ, $R_{22} = 2$ kΩ and $R_3 = 30$ Ω.

Solution:

The gain is:

$$A_V = -(\frac{R_{21} + R_{22}}{R_1} + \frac{R_{22} \cdot R_{21}}{R_1 \cdot R_3})$$

$$A_V = -(\frac{3 + 2}{5} + \frac{2 \cdot 3}{5 \cdot 0.03})$$

$$A_V = -41$$

A inverting voltage follower (A_V = - 1) is shown in Fig.4.47. The input voltage cannot be connected directly to the inverting input, because then it would cancel the negative feedback, and the circuit would behave as a simple comparator. A resistor R thus needs to be connected between v_I and v^-, and an equal sized resistor R between v_O and v^-.

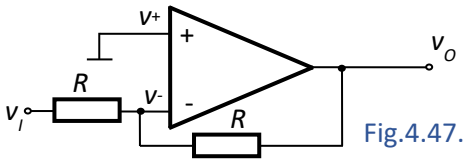


Fig.4.47. Inverting voltage follower

$$v_D = 0\ \text{V} \Rightarrow v^+ = v^-$$

$$v^+ = 0$$

$$v^- = \frac{R}{R+R} \cdot v_O + \frac{R}{R+R} \cdot v_I$$

$$\frac{R}{R+R} \cdot v_O = -\frac{R}{R+R} \cdot v_I$$

$$A_v = -\frac{R}{R} = -1$$

An adjustable gain can be obtained by connecting a potentiometer in series with either R_1 or R_2. The circuit in Fig.4.48 shows an inverting amplifier with adjustable gain, where the potentiometer is connected between the two resistors.

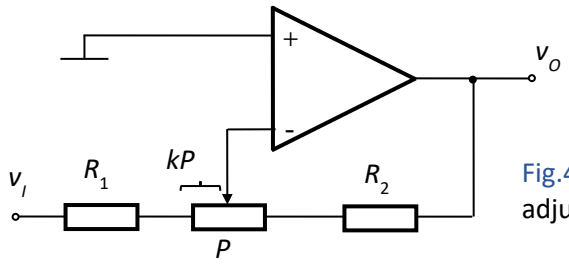


Fig.4.48. Inverting amplifier with adjustable gain

The circuit's equations are:

$$v_D = 0\ \text{V} \Rightarrow v^+ = v^-$$

$$v^+ = 0$$

$$v^- = \frac{R_1 + kP}{R_1 + R_2 + P} \cdot v_O + \frac{R_2 + (1-k)\cdot P}{R_1 + R_2 + P} \cdot v_I$$

$$\frac{R_1 + kP}{R_1 + R_2 + P} \cdot v_O = -\frac{R_2 + (1-k)\cdot P}{R_1 + R_2 + P} \cdot v_I$$

$$A_v = \frac{v_O}{v_I} = -\frac{R_2 + (1-k)\cdot P}{R_1 + kP}$$

$$k = 0 \Rightarrow |A_{vmax}| = \frac{R_2 + P}{R_1}$$

$$k = 1 \Rightarrow |A_{vmin}| = \frac{R_2}{R_1 + P}$$

The minus sign in the expression of the gain shows that the input and output signals are in anti-phase (a positive input results in a negative output, and vice versa). The maximum gain (absolute

value) is obtained for $k = 0$, when the tap of the potentiometer is at the extreme left, whereas the minimum gain (absolute value) is obtained for $k = 1$, extreme right position for the tap of the potentiometer.

Examples

1. Design and size a noninverting amplifier with $A_V = 6$, differential supply of ± 12 V. Deduce and plot the VTC $v_O(v_I)$ for $v_I(t) = 4\sin\omega t$ [V][Hz]. What is the active region of the amplifier? Plot $v_I(t)$ and $v_O(t)$ for:
i) $v_I(t) = 1.5\sin\omega t$ [V][Hz]
ii) $v_I(t) = 4\sin\omega t$ [V][Hz].

Solution:
The circuit to size is the one in Fig.4.37. Using the same notations for the resistors, the gain is:

$$A_v = \frac{v_O}{v_I} = 1 + \frac{R_2}{R_1}$$

$$1 + \frac{R_2}{R_1} = 6$$

$$R_2 = 5 \cdot R_1$$

Any two resistors that meet the above criterion can be chosen. A sample pair of values is:

$$R_1 = 2.5\ \text{k}\Omega \Rightarrow R_2 = 12.5\ \text{k}\Omega$$

The VTC $v_O(v_I)$ is shown in Fig.4.49.

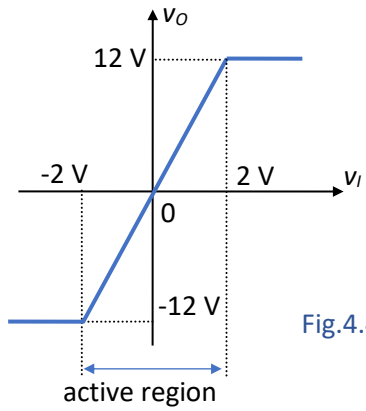
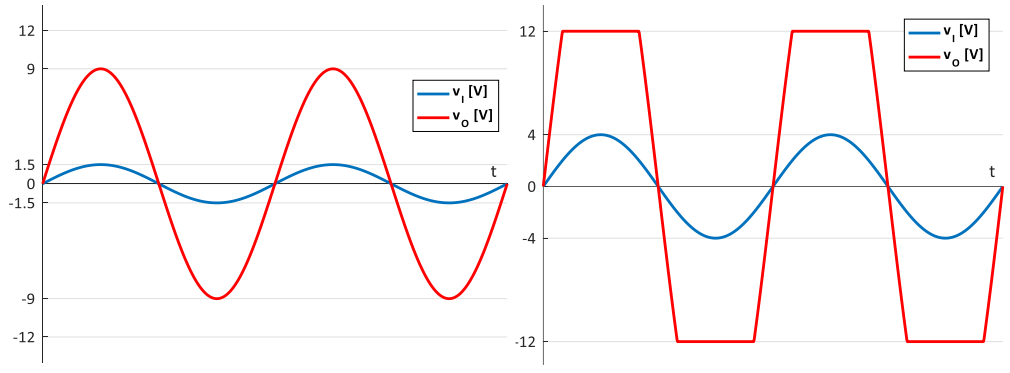


Fig.4.49. VTC $v_O(v_I)$ for the noninverting amplifier



a) b)

Fig.4.50. Waveforms for $v_I(t)$ and $v_O(t)$
a) $v_I(t) = 1.5\sin\omega t$ [V][Hz]; b) $v_I(t) = 4\sin\omega t$ [V][Hz].

The active region is:

$$v_I \in [\frac{-12}{6}; \frac{12}{6}] \text{ [V]}$$
$$v_I \in [-2 \text{ V}; 2 \text{ V}]$$

The waveforms for $v_I(t)$ and $v_O(t)$ are shown in Fig.4.50.
For $v_I(t) = 4\sin\omega t$ [V][Hz], the output voltage is limited by the positive and negative power supplies.

2. For the circuit in **Problem 1**, draw the model of the amplifier.

Solution:
To model the amplifier using a voltage-controlled voltage source, the input and output resistances must be determined:

$$R_i = \frac{v_i}{i_I} = \frac{v^+}{i^+} = \frac{v^+}{0} = \infty$$
$$R_o = \frac{v_{Oopen}}{i_{Osc}} = \frac{v_{Oopen}}{\infty} = 0$$

The model of the amplifier is shown in Fig.4.51.

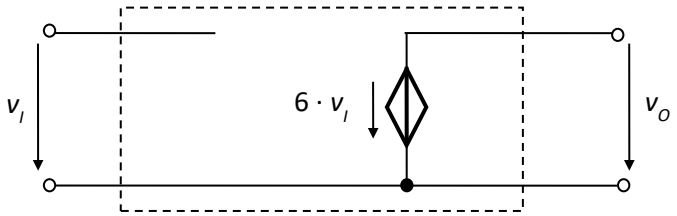


Fig.4.51. Model of the noninverting amplifier

3. Design and size an inverting amplifier with $A_V = -4$, differential supply of ± 12 V. Deduce and plot the VTC $v_O(v_I)$ for $v_I(t) = 4\sin\omega t$ [V][Hz]. What is the active region of the amplifier? Plot $v_I(t)$ and $v_O(t)$ for:
i) $v_I(t) = 1.5\sin\omega t$ [V][Hz]
ii) $v_I(t) = 4\sin\omega t$ [V][Hz].
Compute the input resistance of the amplifier.

Solution:
The circuit to size is the one in Fig.4.43. Using the same notations for the resistors, the gain is:

$$A_v = \frac{v_O}{v_I} = -\frac{R_2}{R_1}$$
$$-\frac{R_2}{R_1} = -4 \Rightarrow R_2 = 4 \cdot R_1$$

Any two resistors that meet the above criterion can be chosen. A sample pair of values is:

$$R_1 = 5 \text{ k}\Omega \Rightarrow R_2 = 20 \text{ k}\Omega$$

The input resistance is equal to R_1.

$$R_i = R_1$$

The VTC $v_O(v_I)$ is shown in Fig.4.52. The active region is:

$$v_I \in [\frac{12}{-4}; \frac{-12}{-4}]\ [V]$$
$$v_I \in [-3\ V; 3\ V]$$

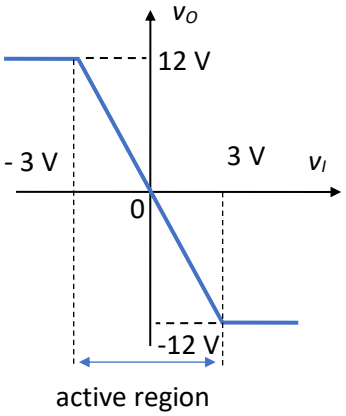


Fig.4.52. VTC $v_O(v_I)$ for the inverting amplifier

The model of the amplifier is presented in Fig.4.53 and the waveforms for $v_I(t)$ and $v_O(t)$ are shown in Fig.4.54.

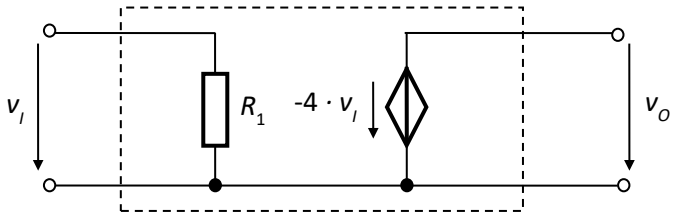


Fig.4.53. Model of the inverting amplifier

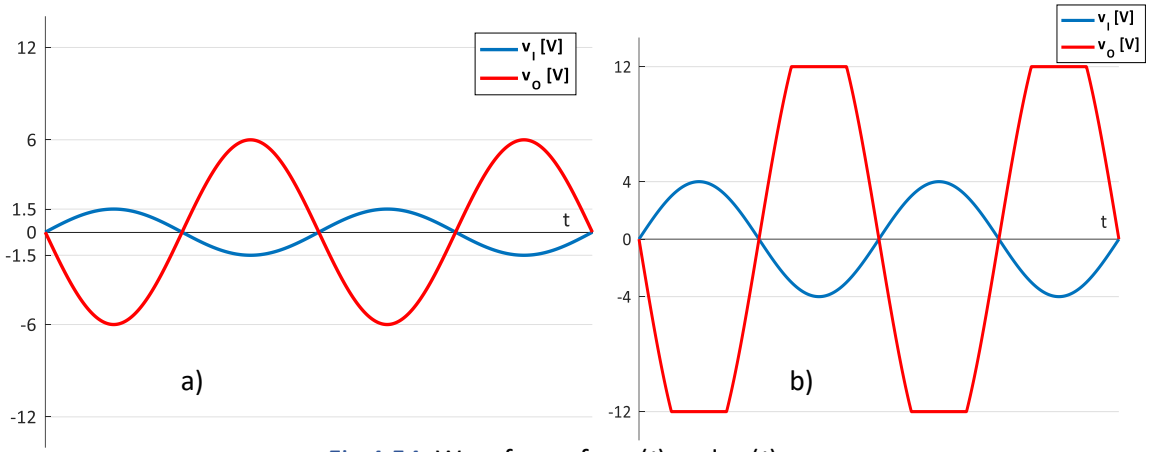


Fig.4.54. Waveforms for $v_I(t)$ and $v_O(t)$
a) $v_I(t)$ = 1.5sinωt [V][Hz]; b) $v_I(t)$ = 4sinωt [V][Hz].

4. Design and size an inverting amplifier with adjustable gain, $A_v \in [-17; -2]$.

Solution:
The circuit is the one in Fig.4.48, and the extreme values of the gain are computed as:

$$|A_{vmax}| = \frac{R_2 + P}{R_1} \Rightarrow 17 = \frac{R_2 + P}{R_1}$$
$$|A_{vmin}| = \frac{R_2}{R_1 + P} \Rightarrow 2 = \frac{R_2}{R_1 + P}$$

The value of P is chosen first, since there are fewer standard potentiometer values. For $P = 5$ kΩ, the equations become:

$$17 = \frac{R_2 + 5}{R_1} \Rightarrow R_2 + 5 = 17 \cdot R_1$$
$$2 = \frac{R_2}{R_1 + 5} \Rightarrow R_2 = 2 \cdot R_1 + 10$$

$$R_2 = 17 \cdot R_1 - 5$$

The values of the two resistors are computed as:

$$17 \cdot R_1 - 5 = 2 \cdot R_1 + 10$$
$$15 \cdot R_1 = 15$$
$$R_1 = 1 \text{ k}\Omega$$
$$R_2 = 12 \text{ k}\Omega$$

The values of the components are $P = 5$ kΩ; $R_1 = 1$ kΩ, $R_2 = 12$ kΩ.

There are other solutions to obtain an amplifier with adjustable gain, such as the one in Fig.4.55, where P is on the negative feedback loop, in series with resistor R_2.
The general expression of the gain is:

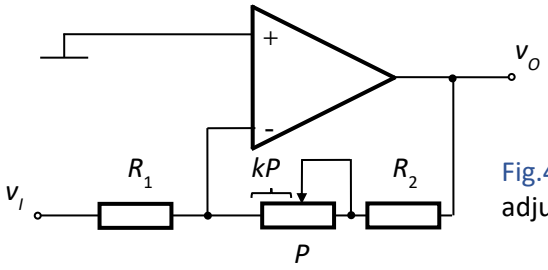


Fig.4.55. Inverting amplifier with adjustable gain – alternative solution

$$A_v = \frac{v_O}{v_I} = -\frac{R_2 + kP}{R_1}$$
$$|A_{vmax}| = \frac{R_2 + P}{R_1} \Rightarrow 17 = \frac{R_2 + P}{R_1}$$
$$|A_{vmin}| = \frac{R_2}{R_1} \Rightarrow 2 = \frac{R_2}{R_1}$$

The equations that determine the values of the resistors are:

$$R_2 + P = 17 \cdot R_1$$
$$R_2 = 2 \cdot R_1$$

The value of P is chosen first, and then the two resistors are sized.

$$2 \cdot R_1 + P = 17 \cdot R_1 \Rightarrow P = 15 \cdot R_1$$

For $P = 5$ kΩ, the closest standard values for the two resistors are $R_1 = 332$ Ω and $R_2 = 665$ Ω. Note that these values are significantly different than the ones determined for the first solution, the circuit in Fig.4.48.

The extreme values of the gain are checked:

$$|A_{vmax}| = \frac{R_2 + P}{R_1} = \frac{0.665 + 5}{0.332} = \frac{5.665}{0.332} = 17.063$$

$$|A_{vmin}| = \frac{R_2}{R_1} = \frac{0.665}{0.332} = 2.003$$

Considering the tolerances of the components, it is considered that the proposed set of values meets the requirements.

A third possible solution is to connect the potentiometer in series with R_1.

Problems

1. Design and size a noninverting amplifier with $A_V = 5$, differential supply of ± 15 V. Deduce and plot the VTC $v_O(v_I)$ for $v_I(t) = 8\sin\omega t$ [V][Hz]. What is the active region of the amplifier? Plot $v_I(t)$ and $v_O(t)$ for $v_I(t) = 8\sin\omega t$ [V][Hz]. Draw the model of the amplifier.

2. Design and size an inverting amplifier with $A_V = -8$, differential supply of ± 10 V. Deduce and plot the VTC $v_O(v_I)$ for $v_I(t) = 3\sin\omega t$ [V][Hz]. What is the active region of the amplifier? Plot $v_I(t)$ and $v_O(t)$ for $v_I(t) = 3\sin\omega t$ [V][Hz]. Draw the model of the amplifier.

3. Design and size an inverting amplifier with adjustable gain, $A_v \in [-10; -4]$. Prove that the gain is adjustable within the specified range.

4. Design and size an amplifier with adjustable gain, $A_v \in [-5; -1]$. Prove that the gain is adjustable within the specified range.

5. Design and size an amplifier with adjustable gain, $A_v \in [1; 8]$. Prove that the gain is adjustable within the specified range.

6. Design and size two possible versions of an amplifier with adjustable gain, $A_v \in [10; 50]$.

7. Design and size an inverting amplifier with adjustable gain, $A_v \in [2; 12]$. For $v_I(t) = 3\sin\omega t$ [V][Hz] and A_{Vmax}, deduce and plot the VTC $v_O(v_I)$, plot $v_I(t)$ and $v_O(t)$. What is the active region of the amplifier? Compute the input and output resistances.

8. Design and size an inverting amplifier with adjustable gain, $A_v \in [-12; -2]$. For $v_I(t) = 1.5\sin\omega t$ [V][Hz] and $A_V = -12$, deduce and plot the VTC $v_O(v_I)$, plot $v_I(t)$ and $v_O(t)$. What is the active region of the amplifier? Compute the input and output resistances.

4.3.3 Summing amplifier

When two or more input voltages are connected at the same input of the op-amp, the circuit is called *summing amplifier*. If the input voltages are connected to the inverting/noninverting input, the circuit is an *inverting/a noninverting summing amplifier*.

A noninverting summing amplifier with two input voltages is shown in Fig.4.56. To find the expression of v^+, the superposition method or Millman's method can be employed, knowing that no currents are drawn by the inputs of the op-amp.

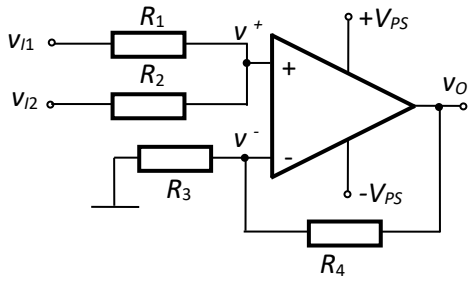


Fig.4.56. Noninverting summing amplifier with two input voltages

The circuit's equations are:

$$\text{NF} \Rightarrow v_D = 0\ \text{V};\ v^+ = v^-$$

$$v^+ = \frac{R_2}{R_1+R_2}\cdot v_{I1} + \frac{R_1}{R_1+R_2}\cdot v_{I2}$$

$$v^- = \frac{R_3}{R_3+R_4}\cdot v_O$$

$$\frac{R_2}{R_1+R_2}\cdot v_{I1} + \frac{R_1}{R_1+R_2}\cdot v_{I2} = \frac{R_3}{R_3+R_4}\cdot v_O$$

$$v_O = \left(1+\frac{R_4}{R_3}\right)\cdot\left(\frac{R_2}{R_1+R_2}\cdot v_{I1} + \frac{R_1}{R_1+R_2}\cdot v_{I2}\right)$$

Each input voltage appears with a different gain in the expression of the output voltage. If the same gain is required for both input voltages, R_1 must be equal to R_2. The output voltage is then computed as:

$$v_O = \left(1+\frac{R_4}{R_3}\right)\cdot\frac{1}{2}\cdot\left(v_{I1} + v_{I2}\right)$$

The name of the circuit is now obvious, since it amplifies the sum of the input voltages.

Two input resistances can be determined, one for each input voltage. The input resistance seen by v_{I1}, when v_{I2} is set to zero, is:

$$R_{i1} = R_1 + R_2$$

The input resistance seen by v_{I2}, when v_{I1} is set to zero, is:

$$R_{i2} = R_1 + R_2$$

The two input resistances are equal. The output resistance is:

$$R_o = 0\ \Omega$$

A summing amplifier can have more than two input voltages. A noninverting summing amplifier with n input voltages is shown in Fig.4.57.

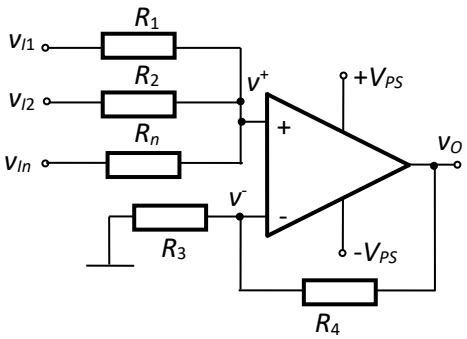


Fig.4.57. Noninverting summing amplifier with n input voltages

To compute the voltage at the noninverting input, either the superposition method (it requires *n* steps) or Millman's method (preferably, since it requires a single step) can be used.

$$v^+ = \frac{\frac{v_{I1}}{R_1} + \frac{v_{I2}}{R_2} + \ldots + \frac{v_{In}}{R_n}}{\frac{1}{R_1} + \frac{1}{R_2} + \ldots + \frac{1}{R_n}}$$

An inverting summing amplifier has two or more input voltages connected to the inverting input of the op-amp. An inverting summing amplifier with two input voltages is shown in Fig.4.58.

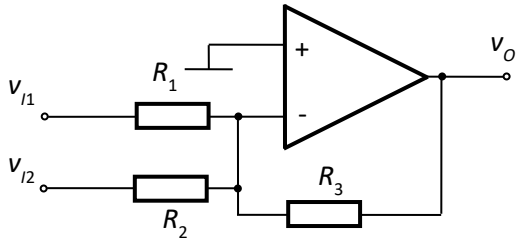


Fig.4.58. Inverting summing amplifier with two input voltages

The circuit's equations are:

$$\text{NF} \Rightarrow v_D = 0\ \text{V};\ v^+ = v^-$$

$$v^+ = 0\ \text{V}$$

$$v^- = \frac{\frac{v_{I1}}{R_1} + \frac{v_{I2}}{R_2} + \frac{v_O}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}} = 0\ \text{V}$$

$$\frac{v_{I1}}{R_1} + \frac{v_{I2}}{R_2} + \frac{v_O}{R_3} = 0$$

$$v_O = -\left(\frac{R_3}{R_1} \cdot v_{I1} + \frac{R_3}{R_2} \cdot v_{I2}\right)$$

To have the same gain for both input voltages, resistors R_1 and R_2 must be equal.

$$R_1 = R_2 = R \Rightarrow v_O = -\frac{R_3}{R} \cdot (v_{I1} + v_{I2})$$

Knowing that $v^- = 0$ V (virtual ground), the input resistances seen by the two input voltages are:

$$R_{i1} = R_1;\ R_{i2} = R_2$$

$$R_o = 0\ \Omega$$

4.3.4 Differential amplifier

The differential amplifier has two input voltages, one connected to the noninverting input, and the other connected to the inverting input, as shown in Fig.4.59.

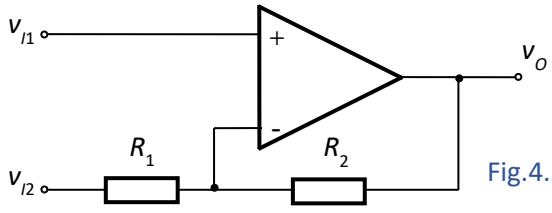


Fig.4.59. Differential amplifier

The circuit's equations are:

$$NF \Rightarrow v_D = 0\ V;\ v^+ = v^-$$

$$v^+ = v_{I1}$$

$$v^- = \frac{R_1}{R_1 + R_2} \cdot v_O + \frac{R_2}{R_1 + R_2} \cdot v_{I2}$$

$$v_{I1} = \frac{R_1}{R_1 + R_2} \cdot v_O + \frac{R_2}{R_1 + R_2} \cdot v_{I2}$$

$$v_O = (1 + \frac{R_2}{R_1}) \cdot v_{I1} - \frac{R_2}{R_1} \cdot v_{I2}$$

The output voltage can also be determined by using the superposition method. The voltage applied at the noninverting input is amplified with a positive factor (the amplifier is noninverting, from the point of view of v_{I1}), and the voltage applied at the inverting input is amplified with a negative factor (the amplifier is inverting, from the point of view of v_{I2}). To obtain an output voltage like $v_O = A_v (v_{I1} - v_{I2})$, the two factors must be equal, in absolute value.

$$\left|1 + \frac{R_2}{R_1}\right| = \left|\frac{R_2}{R_1}\right|$$

This equality cannot be met, regardless of the values of the resistors. The solution is to add a resistive divider for v_{I1}, which means that only a fraction of v_{I1} actually gets to the noninverting input, and only that fraction is to be amplified. The complete schematic is presented in Fig.4.60. The values of the newly added resistors depend on the values of the R_1 and R_2.

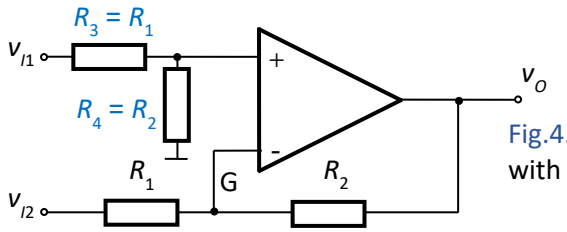


Fig.4.60. Differential amplifier with resistive divider

The voltages v^+ and v_O are computed as:

$$v^+ = \frac{R_4}{R_3 + R_4} \cdot v_{I1}$$

$$v_O = (1 + \frac{R_2}{R_1}) \cdot \frac{R_4}{R_3 + R_4} \cdot v_{I1} - \frac{R_2}{R_1} \cdot v_{I2}$$

If both input voltages need to be amplified with the same factor (absolute value):

$$(1 + \frac{R_2}{R_1}) \cdot \frac{R_4}{R_3 + R_4} = \frac{R_2}{R_1} \Rightarrow \frac{R_4}{R_3 + R_4} = \frac{R_2}{R_1 + R_2}$$

$$\frac{R_3 + R_4}{R_4} = \frac{R_1 + R_2}{R_2}$$

$$1 + \frac{R_3}{R_4} = 1 + \frac{R_1}{R_2} \Rightarrow \frac{R_3}{R_4} = \frac{R_1}{R_2}$$

A special case of the sizing equation is when $R_1 = R_3$ and $R_2 = R_4$, but any values that meet the criterion can be used.

The input resistance seen by v_{I1}, when v_{I2} is set to zero, is:

$$R_{i1} = R_3 + R_4$$

The input resistance seen by v_{I2}, when v_{I1} is set to zero (G is virtual ground), is:

$$R_{I2} = R_1$$

Both input resistances are finite values. The output resistance is 0 Ω.

When $v_{I1} = v_{I2}$, the output voltage is $v_O = 0$ V, meaning that the circuit amplifies the difference between the input voltages, and rejects the common mode signal.

Differential amplifiers are used as instrumentation amplifiers, when a high input resistance and a high common mode rejection ratio is required. The standard instrumentation amplifier is shown in Fig.4.61.

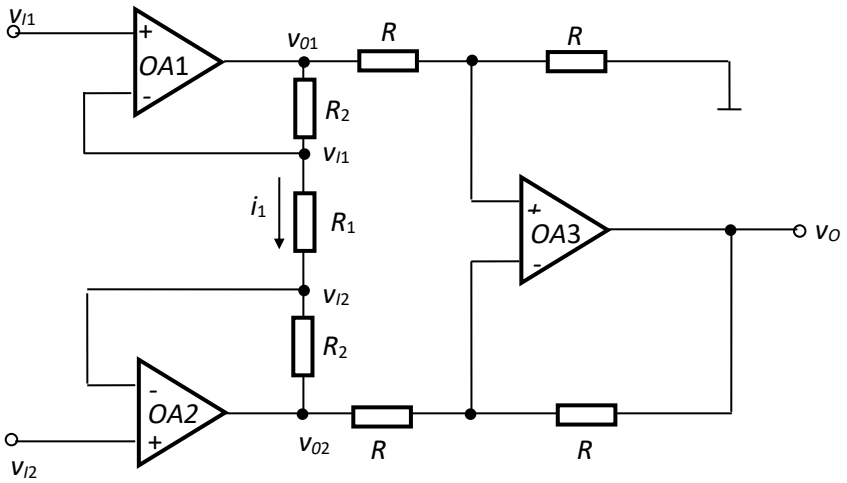


Fig.4.61. Instrumentation amplifier

The highest value of the input resistance is found in the noninverting configuration, and this is the reason why noninverting amplifiers are used for each of the two input voltages. The first amplifier stage is represented by *AO*1 and *AO*2 and it sets the gain, while the second stage, represented by *OA*3, has a unity gain, and ensures the transition from two intermediate output voltages, v_{O1} and v_{O2}, to a single output voltage v_O. The second stage also provides an additional common mode rejection.

The circuit's equations are:

$$v_{O1} = (1 + \frac{R_2}{R_1}) \cdot v_{I1} - \frac{R_2}{R_1} \cdot v_{I2}$$

$$v_{O2} = (1 + \frac{R_2}{R_1}) \cdot v_{I2} - \frac{R_2}{R_1} \cdot v_{I1}$$

$$v_O = (1 + \frac{R}{R}) \cdot \frac{R}{2 \cdot R} \cdot v_{O1} - \frac{R}{R} \cdot v_{O2} = v_{O1} - v_{O2}$$

$$v_O = v_{I1} + \frac{R_2}{R_1} \cdot v_{I1} - \frac{R_2}{R_1} \cdot v_{I2} - v_{I2} - \frac{R_2}{R_1} \cdot v_{I2} + \frac{R_2}{R_1} \cdot v_{I1}$$

$$v_O = v_{I1} + 2 \cdot \frac{R_2}{R_1} \cdot v_{I1} - 2 \cdot \frac{R_2}{R_1} \cdot v_{I2} - v_{I2}$$

$$v_O = v_{I1} - v_{I2} + 2 \cdot \frac{R_2}{R_1} \cdot (v_{I1} - v_{I2})$$

$$v_O = (1 + \frac{2 \cdot R_2}{R_1}) \cdot (v_{I1} - v_{I2})$$

The instrumentation amplifier rejects common mode signals and amplifies the difference between the input voltages. Additionally, the input resistances seen by the two input voltage sources are infinite, which means that the instrumentation amplifier is quite close to an ideal differential amplifier.

4.4 Nonideal properties of the op-amp

For all the circuits presented and analysed so far, it was assumed that the op-amp is ideal. In most applications, this assumption leads to a satisfactory precision of the results. However, there are cases where the nonideal properties of the op-amp can be an issue, especially in integrated circuits.

The nonideal properties are analysed in:

- ac regime (variable signal) – nonideal gain, bandwidth, slew rate, input and output resistances.
- dc regime (biasing) – offset voltage and bias currents.

4.4.1 Nonideal properties in ac regime

Finite voltage gain

The open-loop gain of an op-amp, denoted a, is a finite value (tens, hundreds of thousands). For *OA*741 (most common general-purpose op-amp), the open-loop gain is $a = 200000$.

The VTC $v_O(v_D)$ of the UA741 with differential supply of ±12 V is shown in Fig.4.62. Since UA741 is not a rail-to-rail amplifier, the extreme output voltage is around ±10 V.

$$v_O = a \cdot v_D$$

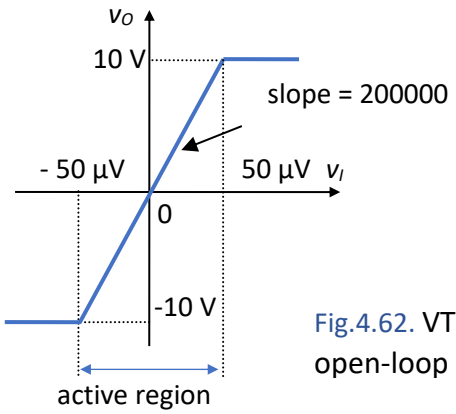


Fig.4.62. VTC $v_O(v_D)$ of a finite open-loop gain amplifier

The active region of the op-amp is [-50 µV; 50 µV], obtained by dividing V_{OH} and V_{OL} to a. The differential input voltage v_D needs to be inside the active region, for the op-amp to work as a voltage amplifier. Outside the active region, the op-amp works as a comparator, when $v_D > 50$ µV and $v_D < -50$ µV.

The finite gain of the op-amp also influences the voltage gain of an amplifier with op-amp. For the noninverting amplifier in Fig.4.63, the voltage gain A_V is a function of the open-loop gain a.

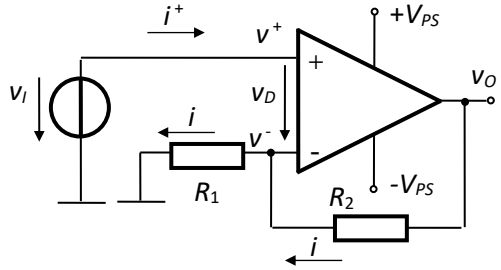


Fig.4.63. Noninverting amplifier

$$v_O = a \cdot v_D$$
$$v_D = v^+ - v^-$$
$$v^+ = v_I$$
$$v^- = \frac{R_1}{R_1 + R_2} \cdot v_O$$
$$v_D = v_I - \frac{R_1}{R_1 + R_2} \cdot v_O$$
$$v_O = a \cdot \left(v_I - \frac{R_1}{R_1 + R_2} \cdot v_O\right)$$

$$A_v = \frac{v_O}{v_I} = \frac{a}{1 + a \cdot \frac{R_1}{R_1 + R_2}}$$

Example

Compute the voltage gain for the noninverting amplifier in Fig.4.63, for R_1 = 4 kΩ and R_2 = 28 kΩ, assuming:
i) $a \to \infty$ (ideal op-amp)
ii) a = 200000 (*OA*741).
Determine the relative and the percent error of the voltage gain considering an ideal op-amp.

Solution:
i) For an ideal op-amp, the voltage gain is:

$$A_{v,\,ideal} = 1 + \frac{R_2}{R_1};\ A_{v,\,ideal} = 8$$

ii) For a nonideal op-amp, the gain is:

$$A_{v,\,a} = \frac{a}{1 + a \cdot \frac{R_1}{R_1 + R_2}}$$
$$A_{v,\,a} = \frac{200000}{1 + 200000 \cdot \frac{4}{32}};\ A_{v,\,a} = 7.9996$$

The difference between the two values is 0.0004 (relative error), and the percent error is:

$$\delta = \left|\frac{A_{v,\,a} - A_{v,\,ideal}}{A_{v,\,ideal}}\right| \cdot 100 = 0.005\%$$

Both the relative and the percent error are smaller than the tolerances of resistors, thus justifying the use of the ideal value of the open-loop gain, when determining the voltage gain of an amplifier with op-amp.

Finite bandwidth

The gain of an op-amp is not constant throughout the entire frequency range, but decreases when the frequency increases. The magnitude response of a general-purpose op-amp is that of a low-pass filter [1], as shown in Fig.4.64. The open-loop gain, $a_O = 10^5$, or 100 dB, and f_O = 10 Hz. The gain decreases with the increase of frequency, the unity gain is obtained at $f_t = 10^6$ Hz.

For unity gain, the op-amp is a voltage follower. Outside the bandwidth, the gain drops 20 dB/decade (for op-amps with internal compensation, which have a capacitor C for frequency compensation). The angular frequencies are:

$$\omega_O = 2 \cdot \pi \cdot f_O \text{ [rad/s]}$$
$$\omega_t = 2 \cdot \pi \cdot f_t \text{ [rad/s]}$$

The complex gain is:

$$A(j\omega) = \frac{a_O}{1 + \frac{j\omega}{\omega_O}}$$

For $\omega >> \omega_O$, the complex gain becomes:

$$A(j\omega) = \frac{a_O \cdot \omega_O}{j\omega}$$

$$|A(j\omega)| = \frac{a_O \cdot \omega_O}{\omega}$$

The unity gain is obtained for ω_t:

$$\omega_t = a_O \cdot \omega_O;\ f_t = a_O \cdot f_O$$

For the noninverting amplifier, the voltage gain is:

$$A_V = 1 + \frac{R_2}{R_1}$$

The -3 dB frequency and the bandwidth is:

$$f_{o,\,Av} = B_{Av} = \frac{f_t}{1 + \frac{R_2}{R_1}} = f_o \cdot \frac{a_o}{1 + \frac{R_2}{R_1}}$$

The bandwidth of a noninverting amplifier with op-amp (negative feedback) is greater than the bandwidth of the op-amp without feedback, but the drawback is the decreased voltage gain.

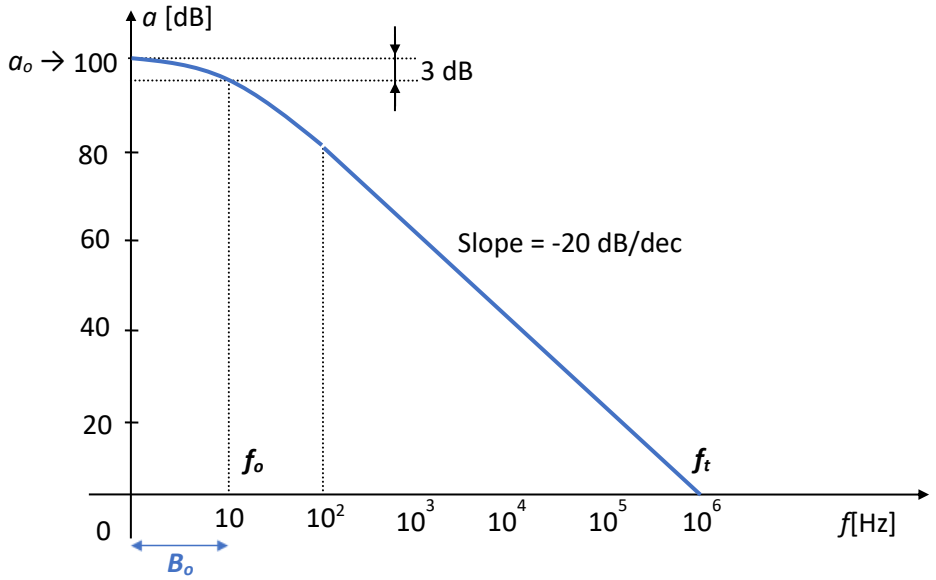


Fig.4.64. Gain-frequency plot of a general-purpose op-amp

Slew rate (SR)

Due to the presence of a frequency compensation capacitor, the output voltage cannot exhibit an instantaneous variation. To exemplify the slew rate of an op-amp, a step signal (Fig.4.65. b) is connected at the noninverting input of a voltage follower Fig.4.65. a).

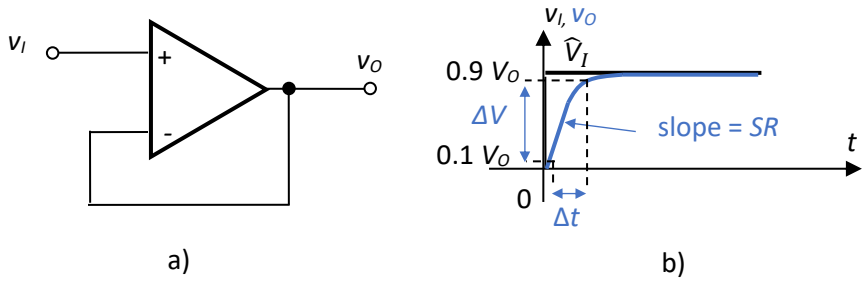


Fig.4.65. Noninverting voltage follower with step input voltage
a) circuit; b) illustration of slew rate

The output voltage does not instantaneously increase from 10% to 90% of the maximum value, but in a finite time, Δt. Between 10% and 90%, the variation of the output voltage is considered linear, and the slope of the segment is the *slew rate* (*SR*) of the op-amp, determined as:

$$SR = \frac{\Delta V}{\Delta t}$$

The slew rate is measured in V/µs and is specified in the datasheet of the op-amp. An ideal op-amp has infinite slew rate. The output voltage can be distorted, due to limitations imposed by the slew rate of the op-amp, even if the voltage is a sine wave - Fig.4.66.

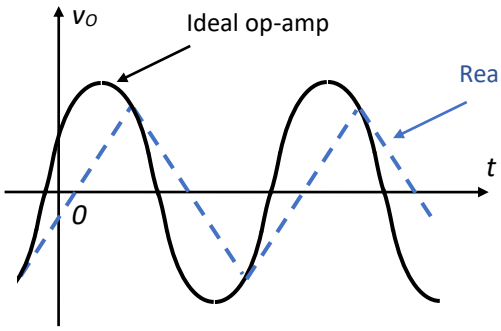


Fig.4.66. Output voltage distorted by finite *SR*

Input and output resistances

For an ideal op-amp, $r_i = \infty$ and $r_o = 0$. For real op-amps, the input and output resistances are finite/non-zero: mega ohms for r_i and tens, hundreds of ohms for r_o. The effects of these real values upon the R_i and R_o of an amplifier with op-amp are analysed on a noninverting amplifier (Fig.4.67).

The input resistance of the amplifier is:

$$R_i = \frac{v_I}{i_I}$$

$$i_I = \frac{v_D}{r_i} = (v_I - \frac{R_1}{R_1 + R_2} \cdot v_O) / r_i$$

$$v_O = a \cdot v_D \Rightarrow R_i = \frac{v_I}{i_I} = r_i (1 + a \cdot \frac{R_1}{R_1 + R_2})$$

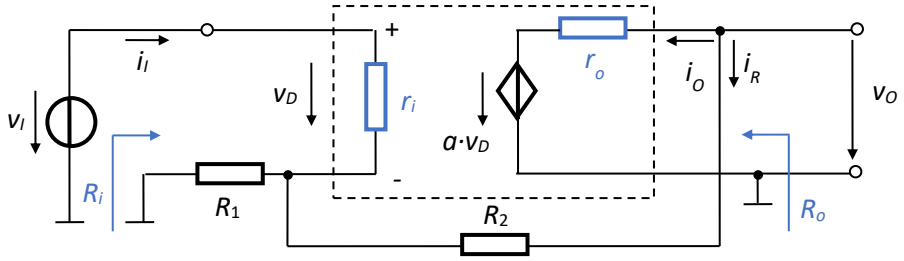


Fig.4.67. Model of the noninverting amplifier

The input resistance of an op-amp with negative feedback, R_i, is greater than the input resistance of the op-amp, r_i, and greater than all other resistances in the circuit. Thus, the effect of negative feedback is to increase the input resistance, bringing it closer to the ideal infinite value.

To determine the output resistance, a test voltage source is applied at the output, and the input voltage is set to zero - Fig.4.68.

$$R_o = \frac{v_{test}}{i_{test}}$$

$$i_{test} = i_2 + i_o = \frac{v_{test}}{R_1 + R_2} + \frac{v_{test} - a \cdot v_D}{r_o}$$

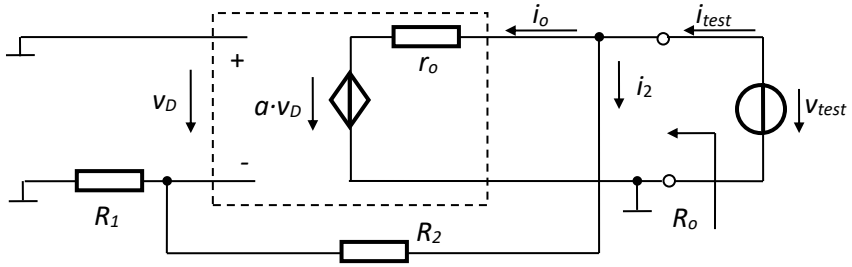


Fig.4.68. Determining the output resistance of the noninverting amplifier

$$v_D = 0 - \frac{R_1}{R_1 + R_2} \cdot v_{test} = - \frac{R_1}{R_1 + R_2} \cdot v_{test}$$

$$R_o = (R_1 + R_2) \,||\, \frac{r_o}{1 + a \cdot \frac{R_1}{R_1 + R_2}} \approx \frac{r_o}{1 + a \cdot \frac{R_1}{R_1 + R_2}}$$

The output resistance of an op-amp with negative feedback, R_o, is smaller than the output resistance of the op-amp, r_o, and smaller than all other resistances in the circuit. Thus, the effect of negative feedback is to decrease the output resistance, bringing it closer to the ideal zero value.

4.4.2 Nonideal properties in dc regime

Offset voltage

For all real op-amps, the output voltage is different from 0 V, when both inputs are connected to 0 V:

$$v^+ = v^- = 0 \text{ V} \Rightarrow v_D = 0 \text{ V, but } v_O = a \cdot v_D \neq 0 \text{ V}$$

The differential voltage that needs to be applied at the input of the op-amp so that the output is 0 V is called the *input offset voltage* (V_{OFF}) and is specified in the datasheet of the op-amp. This voltage

appears as an effect of the fabrication process of the op-amp: the input stages of the op-amp are not perfectly balanced (input currents are not perfectly equal). In general-purpose op-amps, V_{OFF} is a few millivolts, while for precision op-amps, as small as some microvolts (4 µV for MAX400M). The *input offset voltage* can vary in time, due to aging of the components inside the integrated circuit.

Every op-amp has terminals dedicated to offset compensation (*offset null*). Using a potentiometer, it is possible to obtain a 0 V output when both inputs are set to 0 V. Additional circuits for offset compensation can also be used [3].

Reducing the effect of the *input offset voltage* is possible, in some cases, by using capacitive coupling on the negative feedback loop of the op-amp, as shown in Fig.4.69, for a noninverting amplifier.

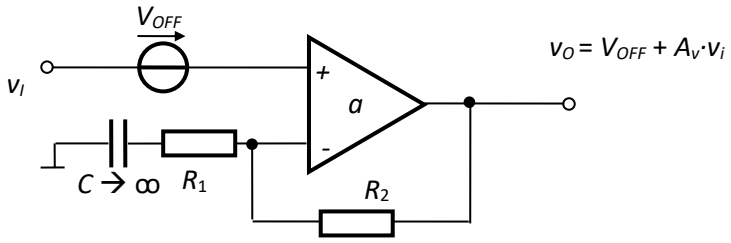


Fig.4.69. Capacitive coupling of the negative feedback loop to reduce the effect of the offset voltage

Bias currents

For the op-amp to properly function, dc currents must flow through its input terminals. These currents are called *input bias currents*, I^+ and I^-.

The average value of these two currents, I_B, is specified in the datasheet of the op-amp, along with their difference, the *offset current*, I_{OFF}.

$$I_B = \frac{I^+ + I^-}{2};\ I_{OFF} = I^+ + I^-$$

For op-amps that have bipolar transistors (BJTs) in the input stage, I_B = 100 nA and I_{OFF} = 10 nA, whereas for op-amps built with field-effect transistors (FETs), I_B is smaller, picoamps.

An amplifier without input voltage is shown in Fig.4.70. For I_B = 100 nA and R_2 = 20 kΩ, if $I^+ = I^-$, the output voltage is:

$$I^+ = I^- = I_B$$
$$V_O = R_2 \cdot I_2 = R_2 \cdot I^- \approx R_2 \cdot I_P \Rightarrow V_O \approx 2\ \text{mV}$$

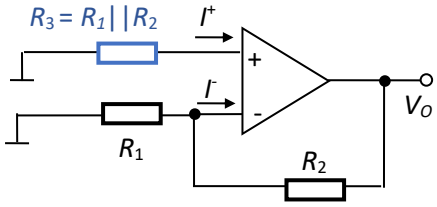


Fig.4.70. Op-amp with negative feedback and bias currents

Although the output voltage determined by the input bias currents is small, there are methods of counteracting this effect, in applications where precision is paramount. One such method is to make sure the same resistance is seen by both inputs of the op-amp, in dc regime, in other words, that the inputs of the op-amp are balanced. For the circuit in Fig.4.70, resistor R_3 was added to the noninverting

input of the op-amp. This newly added component does not influence the amplifier's behaviour in ac regime. Resistor R_3 is the parallel equivalent of resistors R_1 and R_2.

$$V_O = -R_3 \cdot I^+ + R_2 \cdot (I^- - \frac{R_3}{R_1} \cdot I^+)$$

$$V_O = I_B \cdot (-R_3 + R_2 - \frac{R_2 \cdot R_3}{R_1})$$

The output voltage V_O becomes null when:

$$R_3 = \frac{R_1 \cdot R_2}{R_1 + R_2} = R_1 || R_2$$

When the two input bias currents are not equal, the output voltage will no longer be null, but a value determined by the offset current I_{OFF}, much smaller than the output voltage caused by I_B.

$$V_O = R_2 \cdot I_{OFF}$$

4.5 Applications of op-amp amplifiers

From the multitude of applications where the op-amp works as an amplifier (with negative feedback), some of the most important are:

- voltage domain converters – circuits that convert the input voltage range into a different range at the output (e.g., $v_I \in$[2 V; 10 V] is converted to $v_O \in$[3 V; 6 V])
- unipolar supply amplifiers – the op-amp needs additional biasing, so that both the positive and the negative halfwaves of the input voltage are amplified
- precision halfwave and full wave rectifiers – the op-amp is used to build a "superdiode"
- integrators and differentiators – active filters
- capacitively coupled amplifiers – the input voltage has both ac and dc components, and only the ac component (variable) is amplified
- logarithmic and exponential amplifiers, multipliers and division circuits – there is a transistor on the negative feedback loop of the op-amp
- current sources – the generated current is independent of the load resistance
- voltage regulators – the output voltage is constant
- sinusoidal and non-sinusoidal signal generators – circuits with no input voltage, that produce a variable output voltage.

Some of these circuits include transistors, electronic devices that will be discussed in the next chapter. Hence, an in-depth analysis is made for voltage domain converters and unipolar supply amplifiers, whereas the other circuits are only briefly presented.

4.5.1 Voltage domain conversion circuits

A conversion of the voltage domain can be achieved by using either inverting or noninverting voltage amplifiers. The range of values of the input voltage, called *command voltage*, is converted/transformed into a new range of values at the output:

$$v_{cd} \in [V_{cd,min}; V_{cd,max}] \rightarrow v_O \in [V_{O,min}; V_{O,max}]$$
$$V_{cd,min} \neq V_{O,min};\ V_{cd,max} \neq V_{O,max}$$

The range of values for the command voltage can be wider or narrower than the range of values of the output voltage.

Choosing the inverting or noninverting amplifier depends on whether the minimum value of the command voltage leads to a minimum or maximum value of the output voltage. For a noninverting voltage domain converter, the minimum command voltage results in a minimum output voltage:

$$V_{cd,min} \rightarrow V_{O,min};\ V_{cd,max} \rightarrow V_{O,max}$$

For the inverting voltage domain converter, the minimum command voltage will result in a maximum output voltage:

$$V_{cd,min} \rightarrow V_{O,max};\ V_{cd,max} \rightarrow V_{O,min}$$

Converting the voltage domain cannot be achieved without the use of an additional dc voltage source, V_{Ref}, applied at the other input of the op-amp. With one voltage applied to each input, the op-amp operates as a differential amplifier.

A noninverting voltage domain conversion circuit is presented in Fig.4.71. The op-amp is considered to have differential supply, which is not shown on the schematic.

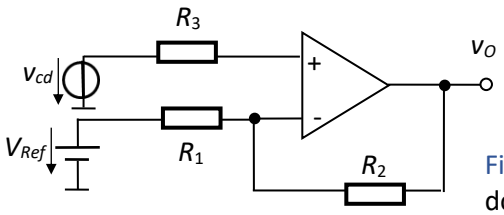


Fig.4.71. Noninverting voltage domain converter

The circuit's equations are:

$$\text{NF} \Rightarrow v_D = 0\ \text{V};\ v^+ = v^-$$

$$v^+ = v_{cd}$$

$$v^- = \frac{R_1}{R_1 + R_2} \cdot v_O + \frac{R_2}{R_1 + R_2} \cdot V_{Ref}$$

$$v_O = \left(1 + \frac{R_2}{R_1}\right) \cdot v_{cd} - \frac{R_2}{R_1} \cdot V_{Ref}$$

For the noninverting configuration, the minimum/maximum command voltage leads to the minimum/maximum output voltage:

$$V_{cd,min} \rightarrow V_{O,min};\ V_{cd,max} \rightarrow V_{O,max}$$

$$V_{O,max} = \left(1 + \frac{R_2}{R_1}\right) \cdot V_{cd,max} - \frac{R_2}{R_1} \cdot V_{Ref}$$

$$V_{O,min} = \left(1 + \frac{R_2}{R_1}\right) \cdot V_{cd,min} - \frac{R_2}{R_1} \cdot V_{Ref}$$

The two equations are solved for V_{Ref} and R_2/R_1. By subtraction, the term that contains V_{Ref} disappears, and the ratio R_2/R_1 is found as a function of the extreme values of the command and output voltages:

$$1 + \frac{R_2}{R_1} = \frac{V_{O,max} - V_{O,min}}{V_{cd,max} - V_{cd,min}} \Rightarrow \frac{R_2}{R_1} = \frac{V_{O,max} - V_{O,min}}{V_{cd,max} - V_{cd,min}} - 1$$

$$V_{Ref} = \frac{(1 + \frac{R_2}{R_1}) \cdot V_{cd,max} - V_{O,max}}{\frac{R_2}{R_1}}$$

Resistor R_3 is sized as the parallel equivalent of resistors R_1 and R_2, as explained in Section 4.4.2:

$$R_3 = R_1 \,||\, R_2$$

The VTC $v_O(v_{cd})$ of a noninverting voltage domain converter is depicted in Fig.4.72. Note the positive slope of the segment, and the fact that only part of the active region is shown (for such circuits, the amplifier doesn't go into saturation).

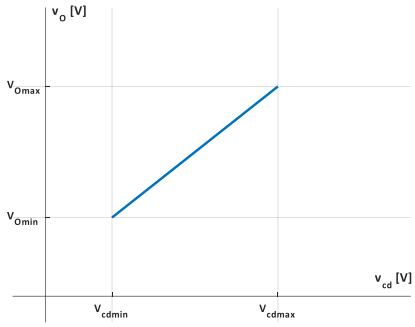


Fig.4.72. VTC $v_O(v_{cd})$ of a noninverting voltage domain converter

For an inverting voltage domain conversion circuit, the command voltage is connected to the inverting input, as seen in Fig.4.73. The circuit's equations are:

$$NF \Rightarrow v_D = 0\ \text{V};\ v^+ = v^-$$

$$v^+ = V_{Ref}$$

$$v^- = \frac{R_1}{R_1 + R_2} \cdot v_O + \frac{R_2}{R_1 + R_2} \cdot v_{cd}$$

$$v_O = (1 + \frac{R_2}{R_1}) \cdot v_{cd} - \frac{R_2}{R_1} \cdot v_{cd}$$

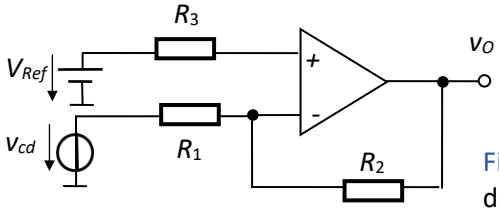


Fig.4.73. Inverting voltage domain converter

For the inverting configuration, the minimum/maximum command voltage leads to the maximum/minimum output voltage:

$$V_{cd,min} \rightarrow V_{O,max};\ V_{cd,max} \rightarrow V_{O,min}$$

$$V_{O,max} = (1 + \frac{R_2}{R_1}) \cdot V_{Ref} - \frac{R_2}{R_1} \cdot V_{cd,min}$$

$$V_{O,min} = (1 + \frac{R_2}{R_1}) \cdot V_{Ref} - \frac{R_2}{R_1} \cdot V_{cd,max}$$

$$\frac{R_2}{R_1} = \frac{V_{O,max} - V_{O,min}}{V_{cd,max} - V_{cd,min}}$$

$$V_{Ref} = \frac{V_{O,min} + \frac{R_2}{R_1} \cdot V_{cd,max}}{1 + \frac{R_2}{R_1}}$$

Resistor R_3 is sized as the parallel equivalent of resistors R_1 and R_2:

$$R_3 = R_1 \,||\, R_2$$

The VTC $v_O(v_{cd})$ of a noninverting voltage domain converter is depicted in Fig.4.74. Note the negative slope of the segment.

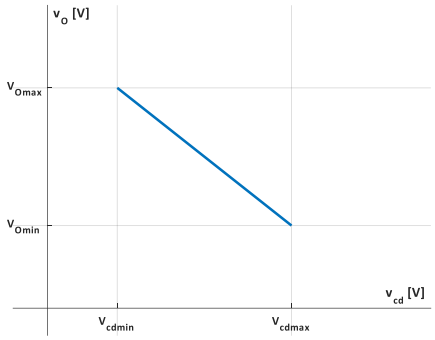


Fig.4.74. VTC $v_O(v_{cd})$ of an inverting voltage domain converter

Example

Design and size a voltage domain convertor, with differential supply ±10 V for which:

$$\begin{Bmatrix} v_{cd} = -4\ V \\ v_O = 3.5\ V \end{Bmatrix}, \begin{Bmatrix} v_{cd} = -1\ V \\ v_O = -2.5\ V \end{Bmatrix}$$

Plot the VTC $v_O(v_{cd})$.

Solution:

The convertor is inverting, based on the requirements ($V_{cd,min}$ determines $V_{O,max,}$ and $V_{cd,max}$ determines $V_{O,min}$) – see Fig.4.73.

$$3.5 = (1 + \frac{R_2}{R_1}) \cdot V_{Ref} - \frac{R_2}{R_1} \cdot (-4)$$

$$-2.5 = (1 + \frac{R_2}{R_1}) \cdot V_{Ref} - \frac{R_2}{R_1} \cdot (-1)$$

The ratio of the two resistors is obtained as:

$$3.5 - (-2.5) = 4 \cdot \frac{R_2}{R_1} - \frac{R_2}{R_1}$$

$$6 = 3 \cdot \frac{R_2}{R_1} \Rightarrow \frac{R_2}{R_1} = 2$$

The voltage V_{Ref} is computed as:

$$3.5 = (1 + 2) \cdot V_{Ref} - 2 \cdot (-4)$$

$$3 \cdot V_{Ref} = -4.5 \Rightarrow V_{Ref} = -1.5\ V$$

Finally, the computed values are replaced in the second equation of the circuit:

$$-2.5 = (1 + 2) \cdot (-1.5) - 2 \cdot (-1)$$

$$-2.5 = -4.5 + 2$$
$$-2.5 = -2.5$$

The equation is verified, meaning the computed values are correct. The resistors must be chosen so that:

$$R_2 = 2 \cdot R_1$$

Any two values that meet the criterion can be chosen, although the values must be in kΩ, to keep the currents small (milliamps). Possible solutions are:

$$S_1: \begin{Bmatrix} R_1 = 5\ k\Omega \\ R_2 = 10\ k\Omega \end{Bmatrix};\ S_2: \begin{Bmatrix} R_1 = 6\ k\Omega \\ R_2 = 12\ k\Omega \end{Bmatrix};\ S_3: \begin{Bmatrix} R_1 = 11\ k\Omega \\ R_2 = 22\ k\Omega \end{Bmatrix};\ S_4: \begin{Bmatrix} R_1 = 4.7\ k\Omega \\ R_2 = 9.4\ k\Omega \end{Bmatrix}$$

The value of R_3 depends on the values of R_1 and R_2. For S_2, the value of R_3 is:

$$R_3 = 6 \,||\, 12 = 4\ k\Omega$$

The final circuit is shown in Fig.4.75.

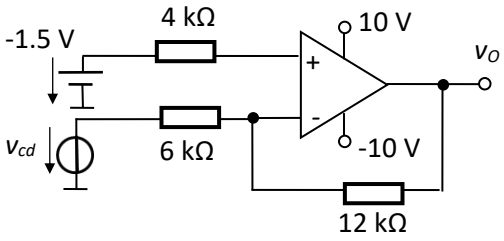


Fig.4.75. Inverting voltage domain convertor – final circuit

The voltage V_{Ref} can be obtained from the negative power supply, using either a resistive divider, or a 1.5 V Zener diode.

The VTC $v_O(v_{cd})$ is shown in Fig. 4.76.

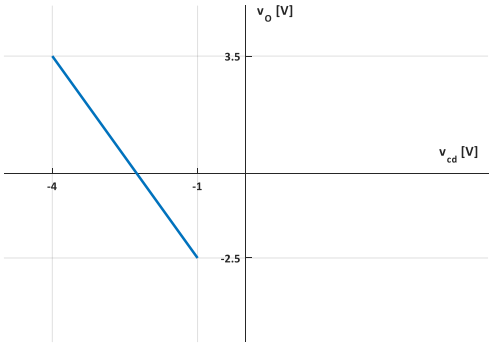


Fig.4.76. VTC $v_O(v_{cd})$ for the proposed inverting voltage domain convertor

Problems

1. Design and size a voltage domain convertor, with differential supply ±10 V for which:

$$\begin{Bmatrix} v_{cd} = -2\ V \\ v_O = 10\ V \end{Bmatrix},\ \begin{Bmatrix} v_{cd} = 1\ V \\ v_O = 4\ V \end{Bmatrix}$$

i) Plot the VTC $v_O(v_{cd})$. What is the value of v_{Cd} for which $v_O = -4$ V?
ii) Propose a schematic to obtain V_{Ref} from the power supply. Size the newly added components.
iii) For $V_{Ref} = 0$ V, deduce and plot the new VTC $v_O(v_{cd})$. What is the new application of the circuit?

2. Design and size a voltage domain convertor, with differential supply ±12 V for which:

$$\begin{Bmatrix} v_{cd} = -2.5\ \text{V} \\ v_O = -13.5\ \text{V} \end{Bmatrix}, \begin{Bmatrix} v_{cd} = 5\ \text{V} \\ v_O = 9\ \text{V} \end{Bmatrix}$$

i) Plot the VTC $v_O(v_{cd})$. What is the value of v_{Cd} for which $v_O = 0$ V?
ii) Propose a schematic to obtain V_{Ref} using a Zener diode. Size the newly added components.
iii) For $V_{Ref} = 0$ V, deduce and plot the new VTC $v_O(v_{cd})$. What is the new application of the circuit?

4.5.2 Amplifiers with unipolar supply

The noninverting amplifier in Fig.4.77 has an input voltage with both ac and dc components. The capacitor C_i, together with resistor R, forms a high pass filter, whose cut-off frequency needs to reject the dc component, and allow all frequencies of the ac component to pass, including the one close to zero frequency.

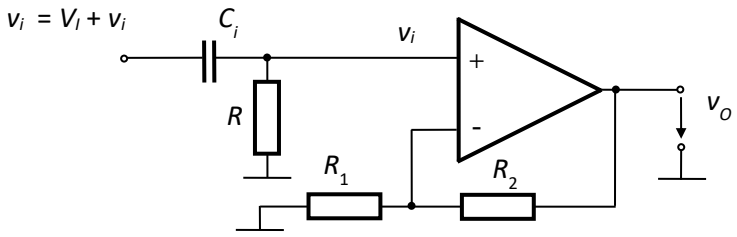


Fig.4.77. Noninverting amplifier with capacitive coupling

The circuit amplifies only the ac (variable) part of the input signal, and the output voltage is only ac. The circuit's equations are:

$$v_I = V_I + v_i$$
$$\text{NF} \Rightarrow v_D = 0\ \text{V};\ v^+ = v^-$$
$$v^+ = v_i$$
$$v^- = \frac{R_1}{R_1 + R_2} \cdot v_o$$
$$v_o = \left(1 + \frac{R_2}{R_1}\right) \cdot v_i$$

For amplifiers with differential supply, both halfwaves (positive and negative) of the input voltage are amplified (the output voltage can be both positive and negative).

If the op-amp is amplified from a single power supply (unipolar supply), positive or negative, the output voltage will only show the positive or negative halfwave. A noninverting single supply amplifier, with positive supply, is shown in Fig.4.78, together with the VTC $v_O(v_I)$ and sample waveforms for $v_I(t)$ and $v_O(t)$.

To amplify the entire input signal, not just the positive halfwave, the solution presented in [4] involves adding to the initial circuit:

- a resistive divider out of the positive power supply, to obtain a dc component that will be added to the variable (ac) input voltage
- two capacitors, to add the ac and dc parts of the input voltage, and to obtain different voltage gains for ac and dc.

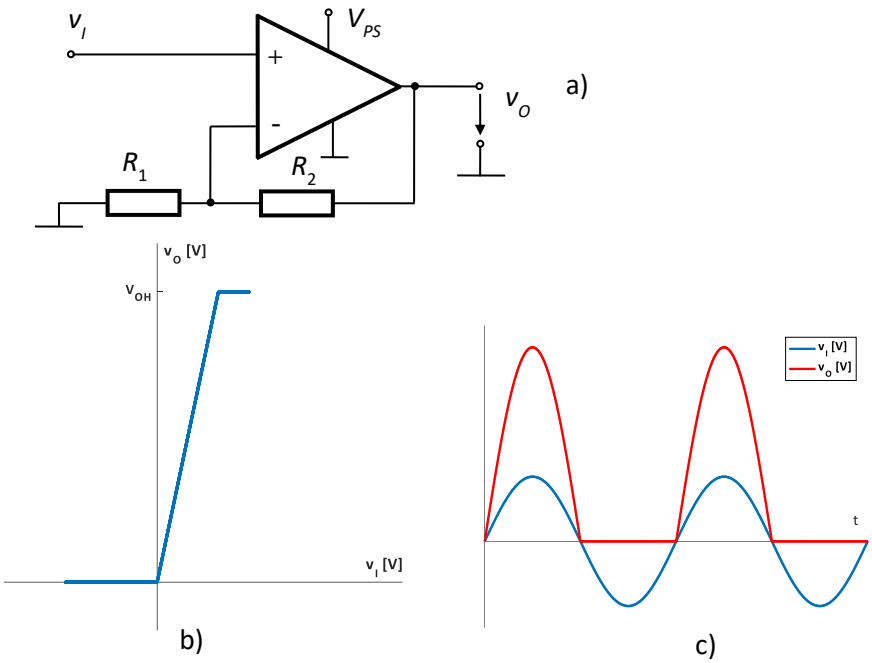


Fig.4.78. Noninverting amplifier with unipolar supply
a) circuit; b) VTC $v_O(v_I)$; c) waveforms for $v_I(t)$ and $v_O(t)$ for op-amp in the active region.

The complete circuit is shown in Fig.4.79. Since the circuit contains capacitors, there will two equivalent circuits, one for dc and one for ac. The voltages seen by the two inputs of the op-amp have ac and dc components.

By adding a dc voltage source V_{Bias} to the variable input voltage v_i, the input voltage is translated towards positive values; this way, the voltage seen at the noninverting input is now only positive.

$$v^+ = v_i + V_{Bias}$$

The ideal value of the dc component is the one for which the maximum active region is obtained. Thus, the ideal value is $V_{Bias} = V_{PS}/2$, and the dc gain is $A_{v,\,dc} = 1$. Capacitor C_1 helps in summing the two components of the voltage connected to the noninverting input, while capacitor C_2 makes the circuit a voltage follower, in dc. The equivalent dc schematic is shown in Fig.4.80, where the two capacitors are considered open circuit.

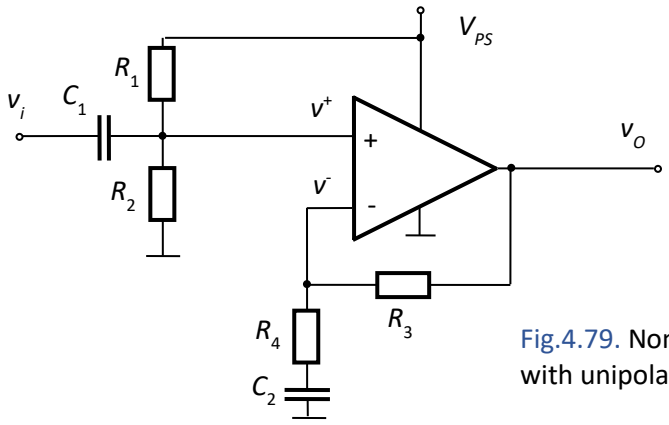


Fig.4.79. Noninverting amplifier with unipolar supply – final circuit

$$\text{NF} \Rightarrow v_D = 0\ \text{V};\ v^+ = v^-$$

$$v^+ = V_{Bias} = \frac{R_2}{R_1 + R_2} \cdot V_{PS}$$

$$\text{For } R_1 = R_2 \Rightarrow V_{Bias} = \frac{V_{PS}}{2}$$

$$v^- = V_O$$

$$V_O = V_{Bias} = \frac{V_{PS}}{2}$$

$$A_{v,\,dc} = \frac{V_O}{V_{Bias}} = 1$$

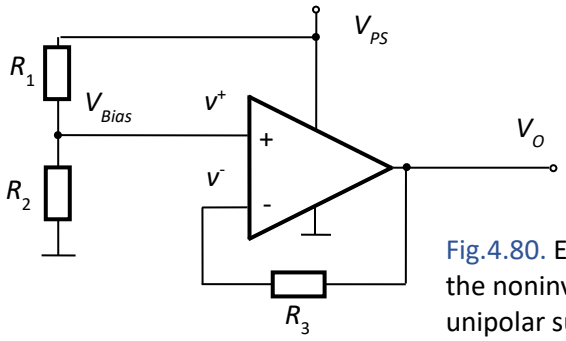


Fig.4.80. Equivalent dc circuit for the noninverting amplifier with unipolar supply

The ac equivalent schematic is shown in Fig.4.81, where the two capacitors are considered short-circuit, and the positive dc power supply V_{Bias} is set to zero. Note that the capacitors cannot be considered short-circuits for any frequency of the input signal; their values must be chosen so that they allow all frequency components of the input signal to pass, even the lowest ones. Resistors R_1 and R_2 have no effect upon the input voltage.

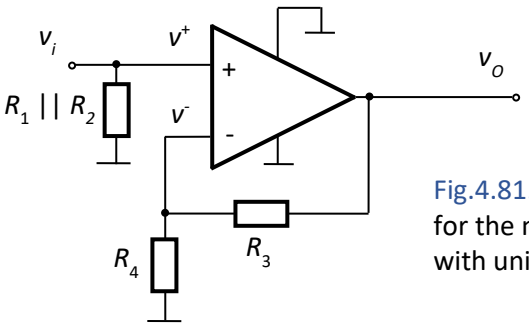


Fig.4.81. Equivalent ac circuit for the noninverting amplifier with unipolar supply

$$\text{NF} \Rightarrow v_D = 0\ \text{V};\ v^+ = v^-$$

$$v^+ = v_i$$

$$v^- = \frac{R_4}{R_3 + R_4} \cdot v_o$$

$$v_o = \left(1 + \frac{R_3}{R_4}\right) \cdot v_i$$

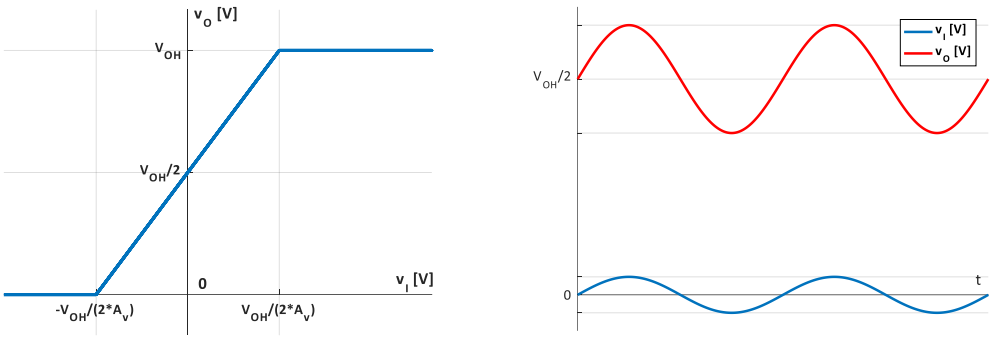
$$A_{v,\,ac} = \frac{v_o}{v_i} = 1 + \frac{R_3}{R_4}$$

Only the variable component of the input voltage is amplified (non-unity gain), while the dc component is amplified with unity gain (voltage follower for dc component). The voltages seen at the

two inputs of the op-amp, v^+ and v^-, are the sum of the voltages seen at the two inputs, in ac and dc regime.

$$v^+ = V_{Bias} + v_i$$
$$v^+ = \frac{V_{PS}}{2} + v_i$$
$$v^- = V_O + \frac{R_4}{R_3 + R_4} \cdot v_o$$
$$v^- = \frac{V_{PS}}{2} + \frac{R_4}{R_3 + R_4} \cdot v_o$$
$$v_O = V_O + v_o$$
$$v_O = A_{v,\,dc} \cdot V_{Bias} + A_{v,\,ac} \cdot v_i$$
$$v_O = 1 \cdot \frac{V_{PS}}{2} + \left(1 + \frac{R_3}{R_4}\right) \cdot v_i$$

The VTC $v_O(v_I)$ and sample waveforms for $v_I(t)$ and $v_O(t)$ are shown in Fig.4.82.



a) b)

Fig.4.82. Noninverting amplifier with unipolar supply
a) VTC $v_O(v_I)$; b) waveforms for $v_I(t)$ and $v_O(t)$ for op-amp in the active region.

The additional components R_1, R_2, C_1, C_2 that appear in the complete circuit shift the VTC $v_O(v_I)$ towards the left, on the horizontal axis, by $V_{PS}/2$; thus, the final circuit will amplify both halfwaves of the input voltage.

The final circuit of an inverting amplifier with unipolar supply is shown in Fig.4.83. The additional components are R_1, R_2, C_1.

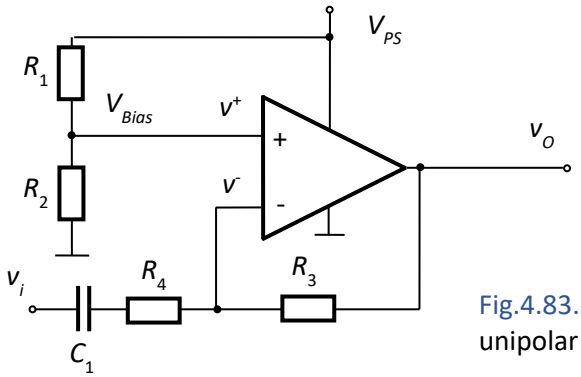


Fig.4.83. Inverting amplifier with unipolar supply – final circuit

The dc equivalent schematic is the same as for the noninverting circuit (Fig.4.80), capacitor C_1 is considered open-circuit, meaning the circuit is a voltage follower in dc.

In the ac equivalent circuit (Fig.4.84), capacitor C_1 is considered short-circuit. A second capacitor is no longer needed, since the voltage seen by the noninverting input is already 0, in ac regime.

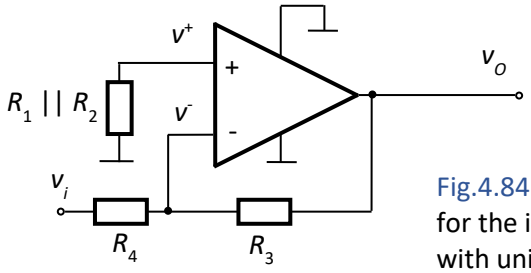


Fig.4.84. Equivalent ac circuit for the inverting amplifier with unipolar supply

$$\text{NF} \Rightarrow v_D = 0\ \text{V};\ v^+ = v^-$$

$$v^+ = 0\ \text{V}$$

$$v^- = \frac{R_4}{R_3 + R_4} \cdot v_o + \frac{R_3}{R_3 + R_4} \cdot v_i$$

$$v_o = \left(-\frac{R_3}{R_4}\right) \cdot v_i$$

$$A_{v,\,ac} = \frac{v_o}{v_i} = -\frac{R_3}{R_4}$$

The voltages seen at the two inputs of the op-amp, v^+ and v^-, are the sum of the voltages seen at the two inputs, in ac and dc regime.

$$v^+ = V_{Bias}$$

$$v^+ = \frac{V_{PS}}{2}$$

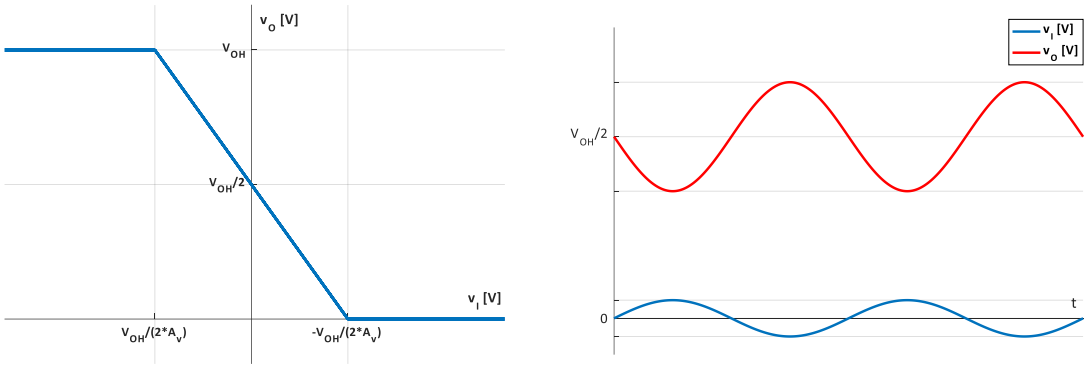
$$v^- = V_O + \frac{R_4}{R_3 + R_4} \cdot v_o + \frac{R_3}{R_3 + R_4} \cdot v_i$$

$$v^- = \frac{V_{PS}}{2} + \frac{R_4}{R_3 + R_4} \cdot v_o + \frac{R_3}{R_3 + R_4} \cdot v_i$$

$$v_O = V_O + v_o$$

$$v_O = A_{v,\,dc} \cdot V_{Bias} + A_{v,\,ac} \cdot v_i$$

$$v_O = 1 \cdot \frac{V_{PS}}{2} + \left(-\frac{R_3}{R_4}\right) \cdot v_i$$



a) b)

Fig.4.85. Inverting amplifier with unipolar supply
a) VTC $v_O(v_I)$; b) waveforms for $v_I(t)$ and $v_O(t)$ for op-amp in the active region.

The VTC $v_O(v_I)$ and sample waveforms for $v_I(t)$ and $v_O(t)$ are shown in Fig.4.85. The additional components R_1, R_2, C_1, that appear in the complete circuit shift the VTC $v_O(v_I)$ towards the left, on the horizontal axis, by $V_{PS}/2$; thus, the final circuit will amplify both halfwaves of the input voltage.

Examples

1. Design and size a single supply amplifier, for which $v_O(t) = -4 \cdot v_I(t) + 8$ V. Justify the type of the amplifier (inverting/noninverting) and determine the value of $V_{PS.}$ Compute $A_{v,\,dc}$ and $A_{v,\,ac}$.

Solution:

The amplifier needs to be inverting, because the coefficient of the variable input voltage is negative (-4) – Fig.4.83. The output voltage is:

$$v_O = A_{v,\,dc} \cdot V_{Bias} + A_{v,\,ac} \cdot v_i$$

$$v_O = 1 \cdot \frac{V_{PS}}{2} + \left(-\frac{R_3}{R_4}\right) \cdot v_i$$

$$v_O(t) = 8 - 4 \cdot v_i(t)$$

$$A_{v,\,dc} = 1;\ A_{v,\,ac} = -4$$

The value of the positive power supply V_{PS} is computed by using the expression of V_{Bias}; the values for R_3 and R_4 are computed from the value of the ac gain.

$$V_{Bias} = \frac{V_{PS}}{2} \Rightarrow R_1 = R_2$$

$$V_{PS} = 2 \cdot V_{Bias} \Rightarrow V_{PS} = 16 \text{ V}$$

$$-\frac{R_3}{R_4} = -4 \Rightarrow R_3 = 4 \cdot R_4$$

Possible values for the four resistors in the circuit are:

$$R_1 = R_2 = 5\ \text{k}\Omega;\ R_3 = 20\ \text{k}\Omega;\ R_4 = 5\ \text{k}\Omega.$$

2. For the circuit designed at **Problem 1**, plot the VTC $v_O(v_I)$, for $v_I \in$ [-5 V, 5 V], and determine the active region of the amplifier. Plot $v_I(t)$ and $v_O(t)$ for $v_I(t) = 1.5\sin\omega t$ [V] and then for $v_I(t) = 4\sin\omega t$ [V].

Solution:

The VTC $v_O(v_I)$ is shown in Fig.4.86. The active region is determined by the extreme values of the input voltage, for which the op-amp works as an amplifier, that is when the output voltage is not clipped. The newly added dc component is half the value of the positive power supply.

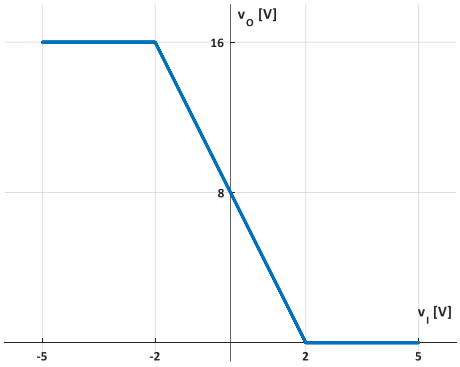


Fig.4.86. VTC $v_O(v_I)$

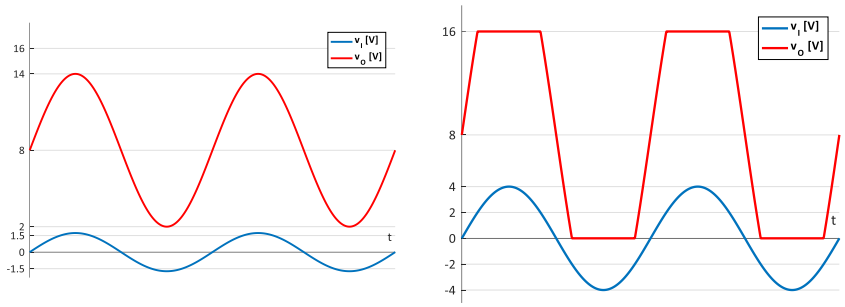
The active region is:

$$v_i \in [\frac{V_{PS}}{2 \cdot A_{v,\,ac}};\ \frac{-V_{PS}}{2 \cdot A_{v,\,ac}}]\ [V]$$

$$v_i \in [\frac{16}{2 \cdot (-4)};\ \frac{-16}{2 \cdot (-4)}]\ [V] \Rightarrow v_i \in [-2;\ 2]\ [V]$$

The waveforms for $v_I(t)$ and $v_O(t)$ for $v_I(t) = 1.5\sin\omega t$ [V] are shown in Fig.4.87. a), and for $v_I(t) = 4\sin\omega t$ [V] in Fig.4.87 b).

For $v_I(t) = 1.5\sin\omega t$ [V], the output voltage is not limited (the input voltage is inside the active region). When the amplitude of v_I is greater than 2 V, the output voltage is limited to a maximum value of 16 V, and a minimum value of 0 V – Fig.4.87 b).



a) b)

Fig.4.87. Waveforms for $v_I(t)$ and $v_O(t)$ for
a) $v_I(t) = 1.5\sin\omega t$ [V]; b) $v_I(t) = 4\sin\omega t$ [V].

Problems

1. Design and size a single supply amplifier for which:

$$v_O(t) = 6 - 5 \cdot v_i(t)$$

Justify the type of the amplifier (inverting/noninverting) and determine the value of V_{PS}. Compute $A_{v,\,dc}$ and $A_{v,\,ac}$.

2. Design and size a single supply amplifier for which:

$$v_O(t) = 6 + 8 \cdot v_i(t)$$

Justify the type of the amplifier (inverting/noninverting) and determine the value of V_{PS}. Compute $A_{v,\,dc}$ and $A_{v,\,ac}$. Plot the VTC $v_O(v_I)$ and determine the active region of the amplifier. Plot $v_I(t)$ and $v_O(t)$ for $v_I(t) = 4\sin\omega t$ [V].

3. Design and size a single supply amplifier for which:

$$v_O(t) = 3 - 5 \cdot v_i(t)$$

Justify the type of the amplifier (inverting/noninverting) and determine the value of V_{PS}. Compute $A_{v,\,dc}$ and $A_{v,\,ac}$. Plot the VTC $v_O(v_I)$. Propose an amplitude for the input voltage, so that the amplifier works in the active region. Plot $v_I(t)$ and $v_O(t)$ for the proposed $v_I(t)$.

4.5.3 Active rectifiers

Active rectifiers are applications of diode circuits. The drawback of diode rectifiers is they are unable to rectify voltages below the threshold voltage of the diode, 0.7 V. Also, the output voltage is always smaller than the input voltage.

A regular diode connected on the negative feedback loop of the op-amp transforms the circuit into a "*superdiode*", for which the threshold voltage is so small, that it can be ignored (microvolts). An active halfwave rectifier, with superdiode is shown in Fig.4.87. The superdiode can be seen as an ideal diode, with 0 V threshold.

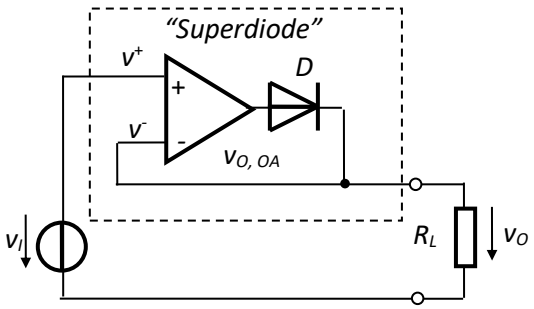


Fig.4.87. Positive halfwave active rectifier with superdiode

The output voltage is determined based on the state of the diode. For $v_{O,\,OA}$ greater than the threshold voltage of the diode, *D* is *on*, and the negative feedback loop of the op-amp is closed.

For $v_{O,\,OA} > 0.7$ V, the op-amp has NF, and $v_D = 0$ V $\Rightarrow v^+ = v^-$

$$v^+ = v_I$$
$$v^- = v_O$$
$$v_O = v_I$$

When $v_{O,\,OA} > 0.7$ V, *D* is *off*, and the op-amp no longer has negative feedback and works as a simple noninverting comparator.

For $v_{O,\,OA} < 0.7$ V, no feedback, and $v_{O,\,OA} = a \cdot v_D$

$$v^+ = v_I$$
$$v^- = 0 \text{ V } (D \text{ - } off)$$
$$v_D = v^+ - v^- = v_I$$
$$v_{O,\,OA} = a \cdot v_I$$
$$v_{O,\,OA} < 0.7 \text{ V} \Rightarrow v_I < \frac{0.7}{a}$$

The open-loop gain of the op-amp is very high, $a = 200000$ for UA741. Because of this high gain, the value of the input voltage for which the op-amp does not have negative feedback can safely be approximated to 0 V.

$$v_I < \frac{0.7}{2 \cdot 10^5} \Rightarrow v_I < 3.5 \text{ µV}$$

For any input voltage $v_I > 3.5$ µV, the op-amp has negative feedback, and works as a voltage follower (the output voltage is equal to the input voltage). The circuit in Fig.4.87 is a positive halfwave active rectifier.

A drawback of active rectifiers with superdiode is given by the time it takes for the op-amp to go from the saturation (passive) region ($v_{O,\,OA} < 0.7$ V) to the active region ($v_{O,\,OA} > 0.7$ V). This delay decreases the speed of the circuit and limits the operating frequency [5].

Full-wave rectifiers can also be built using superdiodes, as shown in Fig.4.88. The circuit is interpreted as a positive halfwave rectifier (*OA*1 and D_1), in parallel with a negative halfwave rectifier (*OA*2, D_2, *R* and *R*).

$v_I > 0$ V; *OA*1 has NF; D_1 – *on*; D_2 – *off*; $v_O = v_I$, given by *OA*1

$v_I < 0$ V; *OA*2 has NF; D_1 – *off*; D_2 – *on*; $v_O = -v_I$, given by *OA*2

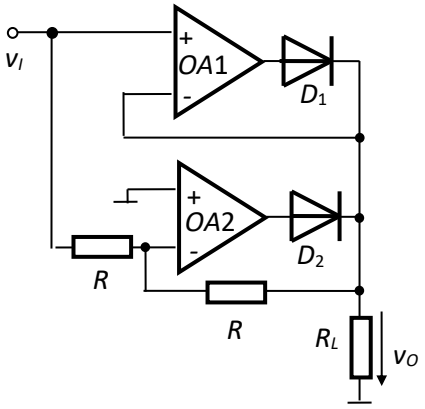


Fig.4.88. Fullwave active rectifier with superdiodes

Active rectifiers with superdiodes are also called *precision rectifiers*: the amplitudes of the input and output voltages are equal, and no voltage is lost on the diode in *on* state.

Superdiodes can replace common diodes in almost any diode circuit.

Chapter 5

TRANSISTORS

In this chapter, you will learn:

- what transistors are and types of transistors
- the operating principle and operating regions of transistors
- the physical structure, operation, and static characteristics of the *n*-type BJT
- the physical structure, operation, and static characteristics of the *n*-type MOSFET
- simple circuits with BJT and MOSFET.

****

5.1 Introduction

The transistor is the third and last electronic device addressed in this book. Alongside diodes and operational amplifiers, transistors are found in almost any electronic circuit.

The transistor can have different functions in different circuits; based on the signal applied to its terminals, the transistor is used either as a switch or as an amplifier.

Transistors are active devices, just like operational amplifiers, with three terminals. In order to operate, transistors need two signal sources – a control or command source (also known as input source), and a power supply. The command or input source is connected between two terminals of the transistor, while the power supply is connected to the third terminal. The input source controls the current flow through the transistor, so the transistor can be modelled using a voltage-controlled current source.

When it comes to the power supply, either dc voltage or dc current sources can be used. The dc voltage source is connected in series with the transistor, while the dc current source requires a parallel connection. Regardless of the type (voltage or current), a resistor needs to be connected in series (for the dc voltage supply) or in parallel (for the dc current supply).

Current trends in circuit design use integrated transistors, with sizes as small as micrometres or even nanometres. The processors that today swiftly bring immense computational power at the tip of our fingers, in computers, mobile phones, smart devices et al, are built using millions and millions of integrated transistors, on a single chip. In computer processors, the transistors operate as switches, and their switching speed impacts the processor's performance.

Moore's law, named after Gordon Moore (1929-2023) – engineer, and co-founder of Intel Corporation, states that the number of transistors on an integrated chip doubles about every two

years [6]. Moore's law proved accurate from 1975 to 1990, but since the 1990s, the transistor count increased slower than predicted. The transistor count on some widely known processors is: Pentium III 1999 – 9.5 million transistors, in 0.25 µm technology; Intel Core I7 4960X 2013 - 1.86 billion transistors, in 22 nm technology [7]. The current highest transistor count is in the Apple M2 Max, with 67 billion transistors, in 5 nm technology [8].

With these immense numbers of integrated transistors in mind, studying the operation and properties of discrete transistors may seem outdated. However, a deep understanding on how transistors work is mandatory for electronics and telecommunications engineers; moreover, there are still many real-life applications where discrete transistors are used.

This chapter starts by describing types of transistors, then addresses the operating regions of transistors in general, and ends with customizing these properties for the BJT and MOSFET.

5.2 Types of transistors

Transistors can be divided into multiple categories, using different criteria (Fig.5.1). Based on the type of carries (electrons or holes) that determine current flow, transistors are:

- *unipolar* or *field-effect transistors* (FETs), where a single type of carriers flowing through a semiconductor channel (*n*-type or *p*-type) determines the current
- *bipolar* or *bipolar junction transistors* (BJTs), where the current flows due to both electrons and holes, through both types of semiconductor material (*n*-type and *p*-type), connected in series. A BJT consists of two *pn* junctions, like the ones discussed in Chapter 2.

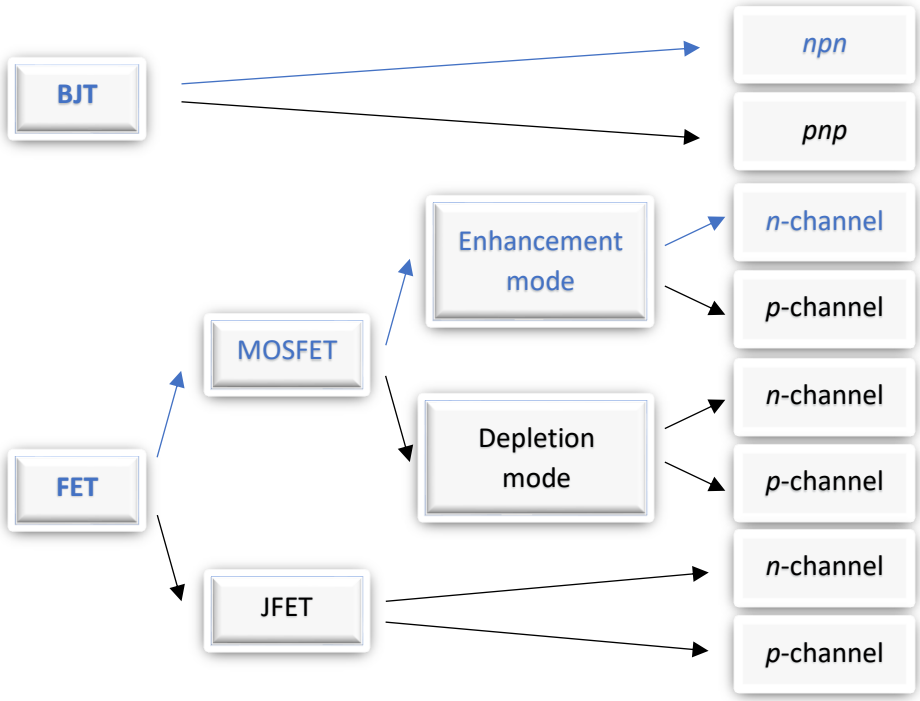


Fig.5.1. Types of transistors

Both FETs and BJTs can be *n*-type or *p*-type:

- for FETs, the current flows through the semiconductor channel, which is either *n*-type or *p*-type, hence the names *n*-type FET or *p*-type FET
- for BJTs, the different ways of connecting the two *pn* junctions results in *n*-type BJT, meaning *npn*, or *p*-type BJT, meaning *pnp*.

Field-effect transistors can be:

- *junction-gate field-effect transistors* – JFET
- *insulated-gate field-effect transistors* (IGFET) or *metal–oxide–semiconductor field-effect transistors* – MOSFET.

Based on the way the semiconductor channel is formed, *n*-channel MOSFETs and *p*-channel MOSFETs can be:

- enhancement mode MOSFETs
- depletion mode MOSFETs.

Out of the eight possible types of transistors, enhancement mode *n*-channel MOSFETs and *npn* BJTs (shown in blue in Fig.5.1) are the most widely used, and this chapter focuses on describing their properties and operation.

5.3 Operating principle and operating regions

Transistors can be modelled as non-linear voltage-controlled current sources (Fig.5.2). The relationship between the current and the control voltage is non-linear: quadratic (square) for MOSFETs and exponential for BJTs. The control voltage V_{CT} determines the current I_T through the transistor (output current). The common terminal for V_{CT} and I_T is marked with an arrow that shows the direction of the positive current flow through the controlled source. The dotted line symbolizes the current through the control terminal (zero for MOSFET and much smaller than I_T for BJT). The circle next to the symbol of the controlled source, for *p*-type transistors, represents the complementary behaviour of the *p*-type transistors, with respect to *n*-type transistors.

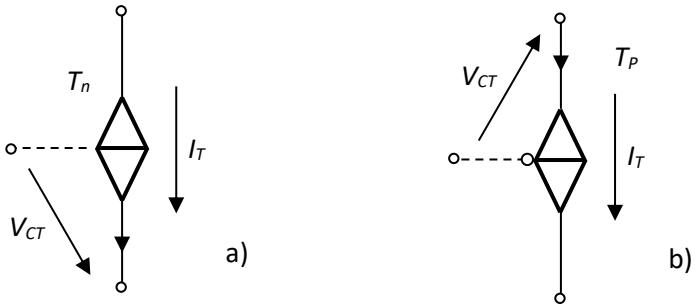


Fig.5.2. Voltage-controlled current source models for transistors
a) *n*-type, T_n; b) of *p*-type, T_p.

Aside from the control voltage v_{CT} and the controlled current i_T (or i_O), the behaviour of the transistors can also be described using the voltage across the transistor v_O and the input (control) current i_I. Thus, three types of static characteristics can be determined:

- input characteristics - the variation of an input variable as a function of another input variable
- output characteristics - the variation of an output variable as a function of another output variable
- transfer characteristics - the variation of an output variable as a function of an input variable.

From the input characteristics in Fig.5.3, one can see that both MOSFETs and BJTs are brought into conduction (*on* state) by applying a control voltage V_{CT} that is above (for *n*-type transistors) or below (for *p*-type transistors) a certain threshold. $V_{Thn} > 0$ is the threshold voltage for *n*-type transistors, while $V_{Thp} < 0$ is the threshold voltage for *p*-type transistors. Once the transistor is *on*, the current I_T through

the third terminal starts to increase, up to a maximum value that is determined by the other components in the circuit (power supply, resistors).

Based on the value of the voltage applied to the command terminal, the four operating regions of the transistor are:

- *cut-off - off*
- *active forward – a_F*
- *extreme conduction – exc*
- *active reverse – a_R* – rarely used.

There is no current flow when the transistor is *off*, and there will be a current flow when the transistor is in a_F, *exc* or a_R, in which case the transistor is said to be *on.*

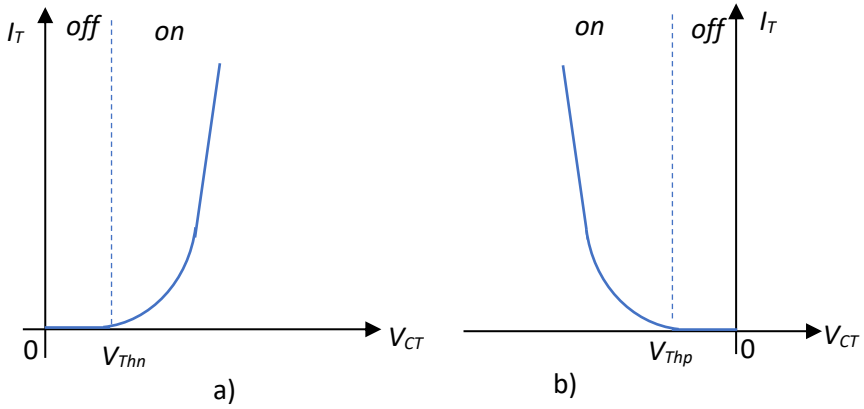


Fig.5.3. Input characteristics $I_T(V_{CT})$
a) T_n; b) T_p.

An *n*-type transistor connected in a circuit with series voltage supply is shown in Fig.5.4. The current through the transistor, I_T, is the same as the output current, I_O. Without resistor *R* in the circuit, the voltage across the controlled source on the transistor would always be equal to V_{PS}.

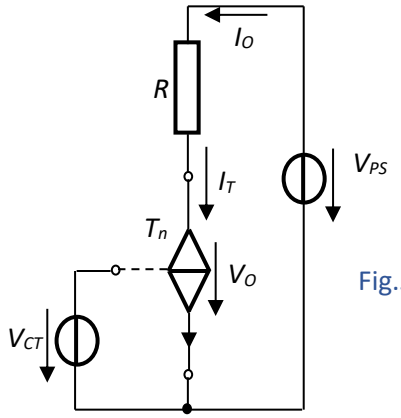


Fig.5.4. T_n in a circuit with series voltage supply

The transfer characteristics $I_O(V_{CT})$ and $V_O(V_{CT})$ are presented in Fig.5.5. The boundary between *off* and a_F is given by V_{Thn}, the threshold voltage of the *n*-type transistor. The boundary between a_F and *exc* is denoted V_{CTex}. The maximum possible value of the current is obtained for T_n in *exc* and is denoted I_{Oex}.

$$V_{CT} > V_{Pn} \Rightarrow T_n \text{ - } on\text{, in either } a_F \text{ or } exc,\ I_O > 0$$
$$V_{CT} > V_{CTex} \Rightarrow T_n \text{ in } exc,\ I_O = I_{Oex}$$

The maximum value of the current is determined by the other components in the circuit: the supply voltage and the resistor. This current can be computed using KVL in the output loop of the circuit:

$$V_{PS} - V_O - I_O \cdot R = 0$$

An increase in the control voltage determines an increase in the output current, which leads to a decrease in the output voltage. Thus, the maximum value of the current, I_{Oex}, is obtained when the output voltage V_O is at the minimum value, that is 0 V.

$$V_O = 0 \text{ V} \Rightarrow I_{Oex} \cdot R = V_{PS}$$
$$I_{Oex} = \frac{V_{PS}}{R}$$

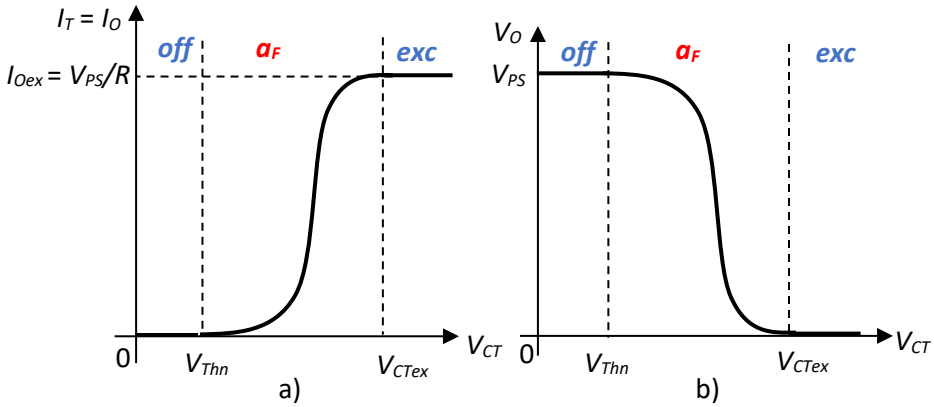


Fig.5.5. Transfer characteristics
a) $I_O(V_{CT})$; b) $V_O(V_{CT})$.

The transfer characteristic $V_O(V_{CT})$ in Fig.5.5. b) is the mirror image of the one in Fig.5.5. a), the evolution of V_O and I_O are opposite (V_O increases/decreases when I_O decreases/increases). The maximum value of the output voltage is obtained when the transistor is *off*, that is when the current I_O is 0 mA.

$$V_{PS} - V_O - I_O \cdot R = 0$$
$$I_O = 0 \text{ mA} \Rightarrow V_{Omax} = V_{PS}$$

The output voltage decreases when T_n enters the a_F region, and reaches a minimum of 0 V when T_n is in *exc*.

To summarize the operation of *n*-type transistors (*npn* BJT and *n*-channel enhancement mode MOSFET):

- the operating region (*off*/a_F/*exc*/a_R) is determined by the value of the control voltage
- when T_n is *off*: $V_{CT} < V_{Thn}$; $I_O = 0$; $V_{Omax} = V_{PS}$
- when T_n is in *exc*: $V_{CT} > V_{CTex}$; $I_{Oex} = \frac{V_{PS}}{R}$; $V_O = 0$
- when T_n is in a_F: $V_{Thn} < V_{CT} < V_{CTex}$; $0 < I_O < I_{Oex}$; $0 < V_O < V_{Omax}$.

The *off* and *extreme conduction* operating regions are considered *passive regions*: the output (current) remains constant when the control (voltage) changes. If the control voltage V_{CT} is set to only have values that keep the transistor in the passive operating regions ($V_{CT} < V_{Thn}$, and $V_{CT} > V_{CTex}$), the transistor operates as a *switch*, or in *switching regime*. If the nonideal properties of the transistor are ignored, a transistor in switching regime acts as an ideal current switch: when the switch is open (*off*), there is no current flow, and when the switch is closed (*on*), the maximum possible current flows through the transistor.

The transistor responds to the changes in the control voltage in the active forward region a_F; here, the current flow through the transistor varies when the control voltage varies. If the control voltage V_{CT} is set to have values that keep the transistor in a_F, that is $V_{CT} \in (V_{Thn}; V_{CTex})$, the transistor operates in *amplification regime.* Note that additional biasing circuitry will be required in this case, to ensure that the quiescent point of the transistor is, ideally, in the middle of the active region.

The boundaries between the three operating regions are determined by the control voltage. The first boundary, between *off* and a_F, is imposed by the transistor itself, through its V_{Thn}. The second boundary, between a_F and *exc,* is V_{CTex}, which depends on the transistor and the other elements of the circuit – supply voltage and resistor.

When it comes to *p*-type transistors (*pnp* BJTs and *p*-channel enhancement mode MOSFETs), they can also be driven to operate in any of the four operating regions (*off*/a_F/*exc*/a_R), by means of the control voltage. Note that the control voltage needs to be below the threshold voltage, for T_p to be *on* (Fig.5.3. b). T_p is used as a *switch* in *off* and *exc*, and as an *amplifier* in a_F.

A *p*-type transistor connected in a circuit with series voltage supply is shown in Fig.5.6. a). The current through the transistor, I_T, is the same as the output current, I_O. Without resistor R in the circuit, the voltage across the controlled source on the transistor would always be equal to V_{PS}. The transfer characteristic $I_O(V_{CT})$ and is presented in Fig.5.6. b). The boundary between *off* and a_F is given by V_{Thp}, the threshold voltage of the *p*-type transistor. The boundary between a_F and *exc* is denoted V_{CTex}. The maximum possible value of the current is obtained for T_p in *exc* and is denoted I_{Oex}.

The operation of *p*-type transistors is:

- when T_p is *off*: $V_{CT} > V_{Thp}$; $I_O = 0$; $V_{Omax} = V_{PS}$
- when T_p is in *exc*: $V_{CT} < V_{CTex}$; $I_{Oex} = \frac{V_{PS}}{R}$; $V_O = 0$
- when T_p is in a_F: $V_{Thp} > V_{CT} > V_{CTex}$; $0 < I_O < I_{Oex}$; $0 < V_O < V_{Omax}$.

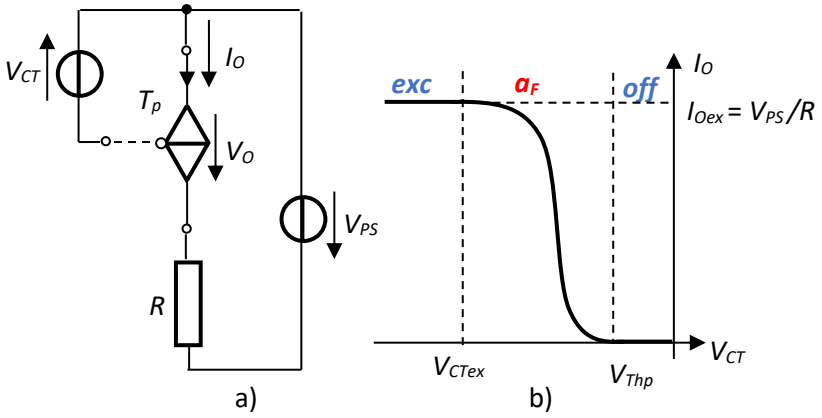


Fig.5.6. *P*-type transistor T_p
a) series voltage supply; b) transfer characteristic $I_O(V_{CT})$.

Example	

Determine the boundaries between the operating regions of T_n and compute I_{Oex} and V_{CTex} for the circuit in Fig.5.4, using the transfer characteristics $I_T(V_{CT})$ in Fig.5.7 and knowing that:
i) V_{PS} = 10 V, R = 1 kΩ;
ii) V_{PS} = 15 V, R = 1 kΩ;
iii) V_{PS} = 10 V, R = 2 kΩ.	

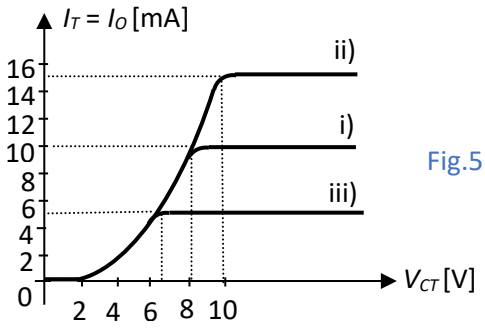


Fig.5.7. Transfer characteristics $I_T(V_{CT})$ for the circuit in Fig.5.4

Solution:

The boundaries between operating regions are identified from the plots, as follows: boundary between *off* and a_F is the first value of V_{CT} for which the current is no longer null ($V_{CT} = V_{Thn}$), while the boundary between a_F and *exc* is the first value of V_{CT} for which the current is at the maximum value ($V_{CTex} = V_{CT}@I_{Oex}$).

The threshold voltage for all three cases is V_{Thn} = 2 V.

The extreme value of the output current can either be computed from the circuit ($I_{Oex} = V_{PS}/R$) or read from the plot.

i) I_{Oex} = 10 mA; V_{CTex} = 8 V

T_n – *off* for $V_{CT} < 2$ V; T_n – a_F for 2 V < $V_{CT} < 8$ V; T_n – *exc* for $V_{CT} > 8$ V;

ii) I_{Oex} = 15 mA; V_{CTex} = 10 V

T_n – *off* for $V_{CT} < 2$ V; T_n – a_F for 2 V < $V_{CT} < 10$ V; T_n – *exc* for $V_{CT} > 10$ V;

iii) I_{Oex} = 5 mA; V_{CTex} = 6.5 V

T_n – *off* for $V_{CT} < 2$ V; T_n – a_F for 2 V < $V_{CT} < 6.5$ V; T_n – *exc* for $V_{CT} > 6.5$ V;

5.4 Bipolar junction transistors (BJTs)

5.4.1 Symbols and physical structure

The bipolar junction transistor BJT has three terminals: base (B), collector (C) and emitter (E). The control voltage is applied between base and emitter, and the controlled current flows through the collector. The symbols for *npn* and *pnp* BJTs are shown in Fig.5.8, where the arrows in the emitter terminal indicate the positive current flow. Since the *npn* BJT is most used, the remainder of this chapter focuses on describing and analysing its behaviour and properties.

Two *pn* junctions form a BJT, and the current flows through both types of semiconductor material (*n* and *p*). For the *npn* BJT (Fig.5.9), the emitter is *n*-type, the base is *p*-type, and the collector is also *n*-type. The emitter is more doped than the collector, hence the n^+ in Fig.5.9 a). The first *pn* junction is between base and emitter. This junction is forward biased when a voltage source is connected between base and emitter (V_{BE} – control voltage) and its value exceeds the threshold value of the *pn* junction $V_{BE,on} \approx 0.6$ V. The second *pn* junction is between base and collector; this junction is reverse biased, because the voltage source connected between collector and emitter (V_{CE} – supply voltage) is much bigger than the control voltage V_{BE}. The *transistor effect* consists in a current flowing through a reverse biased junction (B-C) due to its interaction with a forward biased junction (B-E), placed in its close vicinity.

The *transistor effect* occurs when the following criteria is met simultaneously:

- there are two voltage sources connected to the transistor, a control voltage (V_{BE}) and a supply voltage V_{CE}, and $V_{CE} >> V_{BE}$
- the base region is very thin, considerably thinner than the diffusion length of the minority carriers in the base region
- the emitter region is more doped than the collector and base regions
- the emitter and collector regions are wider than the diffusion length of the minority carriers in these regions.

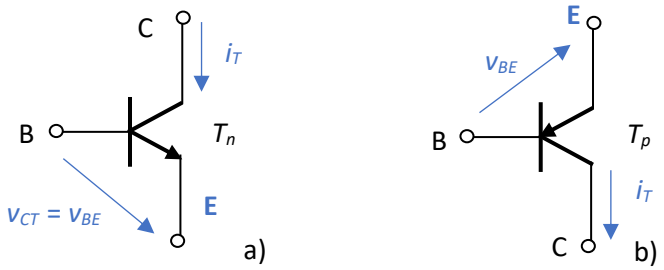


Fig.5.8. Circuit symbols for the BJT
a) *npn*; b) *pnp.*

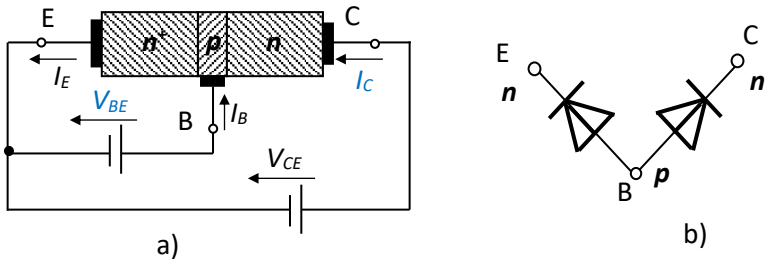


Fig.5.9. *npn* BJT
a) simplified phsyical structure with voltage sources; b) ohmmeter's view.

The current flow that results from the forward bias of the base-emitter junction is consists of electrons injected from the emitter to the base, and holes injected from the base to the emitter, the former being significantly bigger than the latter. A small part of the electrons injected from the emitter will combine with the holes in the base (between 0.5% and 5%), resulting in a *recombination current*. Since the base region is thinner than the diffusion length of the electrons, the majority of electrons are thus able to pass the reverse-biased base-collector region and reach the collector. The current flowing through the reverse-biased base-collector region is called *saturation current* (see Chapter 2), with values small enough to be neglected (units of 10^{-15} A for Silicon transistors).

The BJT is a current node, the emitter current is the sum of the base and collector currents, regardless of the operating region of the transistor:

$$I_E = I_B + I_C$$

The base current is much smaller than the emitter and collector currents, thus the emitter and collector currents are often assumed equal:

$$I_B \ll I_C, I_E \approx I_C$$

An ohmmeter's view of the *npn* BJT, without any applied voltage sources, shows the two *pn* junctions (Fig.5.9. b) [9]. This does not imply that a BJT can be built with or is equivalent to two diodes.

5.4.2 Operation and static characteristics

Although resistors are not present in the schematic proposed in Fig.5.9, when connecting the BJT in a circuit, the current flow through it must be controlled. The two basic ways of controlling the current through the control terminal (base) are shown in Fig.5.10 – using a resistor in the base and limiting the base current (Fig.5.10. a) or using a resistor in the emitter and limiting the emitter current (which includes the base current) (Fig.5.10. b). Circuits where both resistors are present are also possible.

For the circuit in Fig.5.10. a), the base current is determined by the control voltage V_{CT} and resistor R_B:

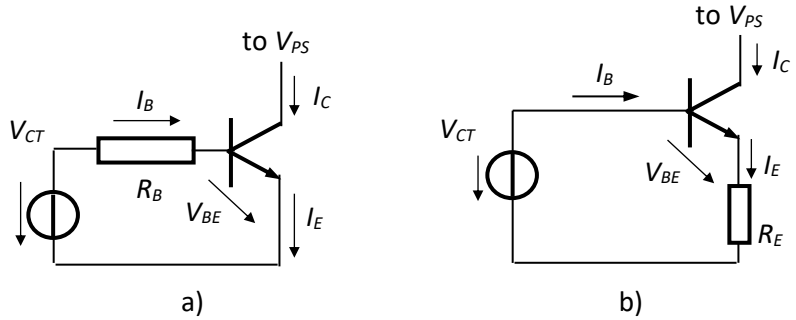
$$V_{CT} - V_{BE} - I_B \cdot R_B = 0$$

$$I_B = \frac{V_{CT} - V_{BE}}{R_B}$$

For the circuit in Fig.5.10. b), the emitter current is determined by the control voltage V_{CT} and resistor R_E:

$$V_{CT} - I_E \cdot R_E - V_{BE} = 0$$

$$I_E = \frac{V_{CT} - V_{BE}}{R_E}$$



a) b)

Fig.5.10. Limiting the control current through the BJT
a) resistor in the base; b) resistor in the emitter.

In practical circuits, the current through the collector is also limited, by connecting another resistor in the collector (Fig.5.11. a) or in the emitter (Fig.5.11. b). Circuits where both resistors are present are also possible.

For the circuit in Fig.5.11. a), the collector current is computed as:

$$V_{PS} - V_{CE} - I_C \cdot R_C = 0$$

$$I_C = \frac{V_{PS} - V_{CE}}{R_C}$$

For the circuit in Fig.5.11 b), the emitter current (which includes the collector current) is computed as:

$$V_{PS} - I_E \cdot R_E - V_{CE} = 0$$

$$I_E = \frac{V_{PS} - V_{CE}}{R_E}$$

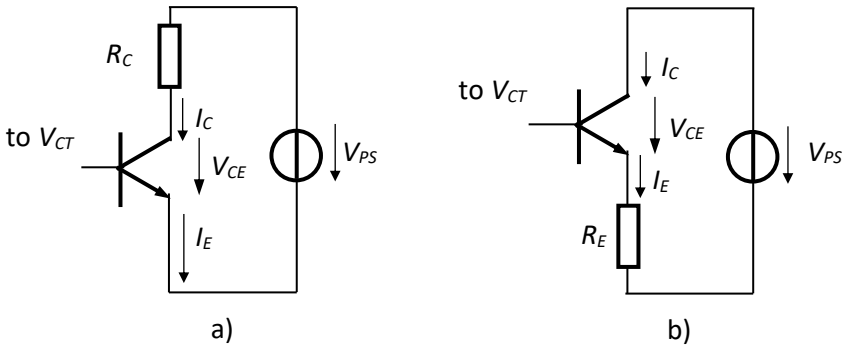


Fig.5.11. Limiting the controlled current through the BJT
a) resistor in the collector; b) resistor in the emitter.

Thus, for the safe operation of a BJT, at least two resistors are required, one to limit the current through the control terminal (base), and the other to limit the controlled current (through the collector). For the circuit in Fig.5.12. a), the resistors are placed in the base and in the collector of the BJT.

The static transfer characteristic depicts the variation of the controlled current i_C as a function of the control voltage, v_{BE} – Fig.5.12. b). The operating regions of the BJT are easily distinguishable:

- *cut-off* (*off*), where $v_{BE} < 0.6$ V and $I_C = 0$ mA
- *active forward* (a_F), where $0.6 \text{ V} < v_{BE} < V_{BEsat}$ and $0 < I_C < I_{Cex}$
- *extreme conduction* or *saturation* (*exc*), where $v_{BE} > V_{BEsat}$ and $I_C = I_{Cex}$.

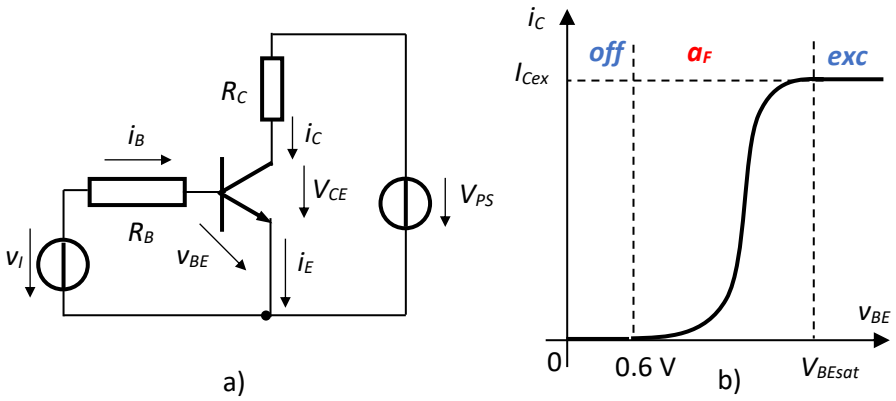


Fig.5.12. Circuit with BJT to determine the static transfer characteristic
a) schematic; b) i_C (v_{BE}).

In *active forward*, the collector current is an exponential function of the control voltage, with the simplified equation seen in Chapter 2 and the thermal voltage V_T is assumed 25 mV at room temperature:

$$i_C = I_S \cdot e^{\frac{v_{BE}}{V_T}}$$

The two *pn* junctions, one in *forward bias* and the other in *reverse bias*, determine a base current i_B when the BJT is *on*. The base current i_B when the BJT is in a_F is computed as:

$$i_B = \frac{I_S}{\beta} \cdot e^{\frac{v_{BE}}{V_T}}$$

$$i_C = \beta \cdot i_B$$

where β is the *forward current gain factor* (also denoted h_{FE} in dc or h_{fe} in ac) and is dimensionless.

In practical circuits, β varies from tens to hundreds, and it depends on V_{CE} and I_C. When computing, β is assumed to be a round value (50, 100, 200), usually β = 100, unless otherwise specified. The static characteristics for the *npn* BJT with $I_S = 2 \cdot 10^{-15}$A and β = 100 are shown in Fig.5.13. For any control voltage v_{BE} < 0.6 V, the BJT is *off* and i_B and i_C are considered 0 mA. When the control voltage exceeds the 0.6 V threshold voltage, the two currents increase exponentially with the increase of v_{BE}. When the BJT is in a_F, the base current i_B and the collector current i_C show and identical variation, but the base current is β = 100 times smaller than the collector current – Fig.5.13. b).

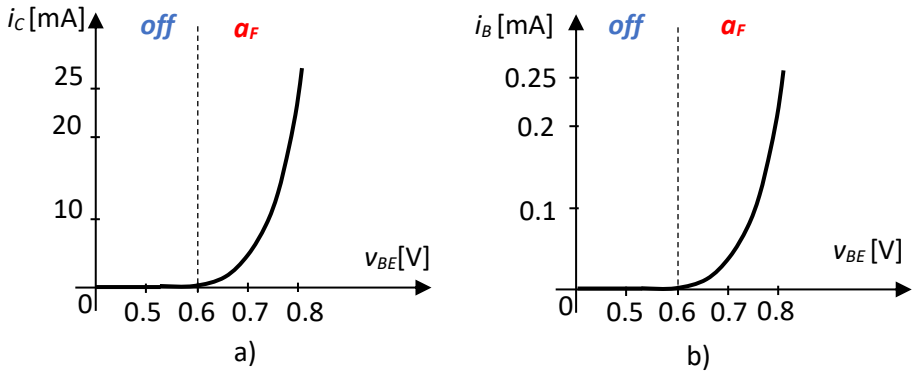


Fig.5.13. Static characteristics for the *npn* BJT
a) transfer; b) input.

The current transfer characteristic $i_C(i_B)$ is shown in Fig.5.14. When the BJT is in a_F, there is a linear relation between the two currents:

$$\text{BJT in } a_F\text{: } i_C = \beta \cdot i_B$$

In *exc*, the collector current is limited to I_{Cex}, even if the base current keeps increasing (the BJT no longer keeps up with the increase of the control current):

$$\text{BJT in } exc\text{: } i_C = I_{Cex} < \beta \cdot i_B$$

The BJT goes into *exc* when the base current is above I_{Bsat}. I_{Bsat} is the limit between a_F and *exc*, and can be seen as the first value of the base current for which the BJT is in *exc,* or the last value for which the BJT is in a_F:

$$I_{Bsat} = \frac{I_{Cex}}{\beta}$$

When the BJT is *off*, both the base and the collector currents are null. This operating region is the origin of the plot in Fig.5.14.

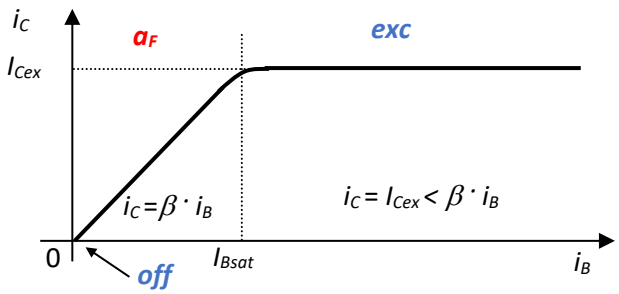


Fig.5.14. Current transfer characteristic $i_C(i_B)$ for the *npn* BJT

In practical circuits, the control voltages are not to have values close to the limits between the operating regions of the BJT ($V_{BE,on}$ and V_{BEsat}). The extreme values of the forward current gain factor β are given in the datasheet of the BJT. For the BJT to operate exclusively in *exc*, the base current must exceed the highest possible value of I_{Bsat}:

$$i_B > I_{Bsat\ max} = \frac{I_{Cex}}{\beta_{min}}$$

For the BJT to operate exclusively in a_F, the base current must be lower than the lowest possible value of I_{Bsat}:

$$i_B < I_{Bsat\ min} = \frac{I_{Cex}}{\beta_{max}}$$

The family of output characteristics $i_C(v_{CE})$ in Fig.5.15 is obtained by varying the control voltage v_{BE} or the control current i_B.

The operating regions of the BJT are easily distinguishable here as well:

- *cut-off* (*off*), where $I_C = 0$ mA (the horizontal axis)
- *active forward* (a_F), where 0.2 V < V_{CE} and 0 < I_C < I_{Cex}
- *extreme conduction* or *saturation* (*exc*), where $v_{CE} = V_{CE,sat} \approx 0.2$ V (close to the vertical axis).

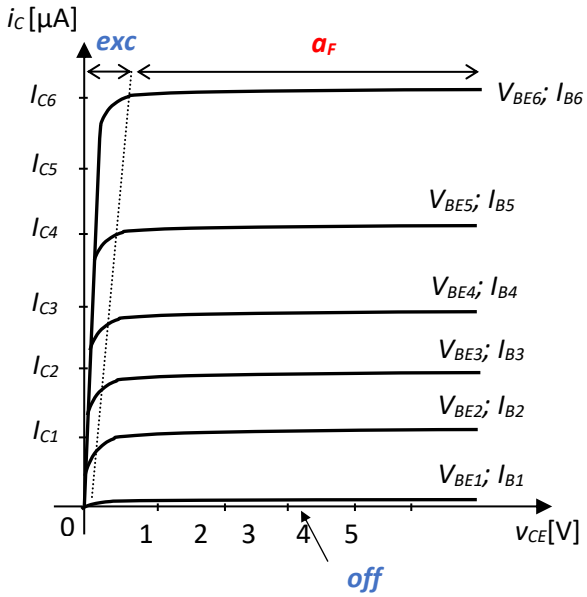


Fig.5.15. Family of output characteristics $i_C(v_{CE})$ for the *npn* BJT

To conclude, the operating regions of the *npn* BJT are:

- *cut-off* (*off*), where the BJT works as an open switch:

$$v_{BE} < V_{BE,on} \approx 0.6\ \text{V};$$
$$I_B = I_C = 0\ \text{mA}$$
$$V_{CE} = V_{PS}$$

- *extreme conduction* or *saturation* (*exc*), where the BJT works as a closed switch:

$$v_{BE} > V_{BEsat};\ I_{Bsat} = \frac{I_{Cex}}{\beta};\ i_B > I_{Bsat}$$

$$I_C = I_{Cex} = \frac{V_{PS} - V_{CEsat}}{R}$$
$$v_{CE} = V_{CEsat} \approx 0.2\ \text{V}$$

- *active forward* (a_F), where the BJT works as an amplifier:

$$V_{BE,on} < v_{BE} < V_{BEsat}$$
$$i_C = I_S \cdot e^{\frac{v_{BE}}{V_T}}$$
$$i_C = \beta \cdot i_B$$
$$i_E = i_B + i_C = (\beta + 1) \cdot i_B$$
$$0 \text{ mA} < i_C < I_{Cex}$$
$$0.2 \text{ V} < V_{CE} < V_{PS}$$

Examples

1. Determine the operating region of T in Fig.5.16, if $V_{BE,on} = 0.6$ V, $\beta = 100$, for the following values of the control voltage V_{CT}:
i) $V_{CT} = 0.3$ V
ii) $V_{CT} = 1.6$ V
iii) $V_{CT} = 7$ V.
Compute the values of I_C and V_{CE} for each case.

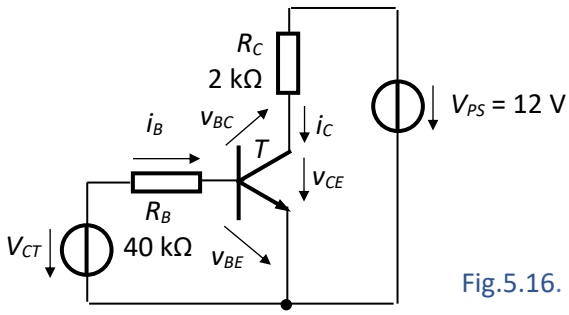


Fig.5.16. BJT circuit

Solution:
i) Since $V_{CT} < V_{BE,on}$, T is *off*.

$$I_B = I_C = 0 \text{ mA}$$
$$V_{CE} = V_{PS} - I_C \cdot R_C$$
$$V_{CE} = V_{PS}$$

ii) In this case, $V_{CT} > V_{BE,on}$, so T is *on,* either in a_F or exc. The idea is to assume T is in one of the two possible operating regions and check that the criteria for that region are met.
Assumming T is in a_F, the currents are computed as:

$$i_B = \frac{V_{CT} - v_{BE}}{R_B} = \frac{1.6 - 0.6}{40 \cdot 10^3} = 0.025 \text{ mA}$$

$$I_{Cex} = \frac{V_{PS} - V_{CEsat}}{R_C} = \frac{12 - 0.2}{2 \cdot 10^3} = 5.9 \text{ mA}$$

$$I_{Bsat} = \frac{i_{Cex}}{\beta} = \frac{5.9 \cdot 10^{-3}}{100} = 0.059 \text{ mA}$$

For a_F, i_B must be lower than I_{Bsat}:

$$0.025 \text{ mA} < 0.059 \text{ mA}$$

or i_C lower than I_{Cex}:

$$i_C = \beta \cdot i_B = 100 \cdot 0.025 \cdot 10^{-3} = 2.5 \text{ mA}$$
$$2.5 \text{ mA} < 5.9 \text{ mA}$$

The criteria are met, meaning the assumption that T is in a_F was correct.
The collector-emitter voltage V_{CE} is computed as:

$$V_{CE} = V_{PS} - I_C \cdot R_C$$

$$V_{CE} = 12 - 2.5 \cdot 10^{-3} \cdot 2 \cdot 10^{3} = 7 \text{ V}$$

iii) The steps employed at ii) are repeated here:

$$i_B = \frac{V_{CT} - v_{BE}}{R_B} = \frac{7 - 0.6}{40 \cdot 10^{3}} = 0.16 \text{ mA}$$

$$I_{Cex} = \frac{V_{PS} - V_{CEsat}}{R_C} = \frac{12 - 0.2}{2 \cdot 10^{3}} = 5.9 \text{ mA}$$

$$I_{Bsat} = \frac{i_{Cex}}{\beta} = \frac{5.9 \cdot 10^{-3}}{100} = 0.059 \text{ mA}$$

The currents i_B and I_{Bsat} are compared:

$$0.16 \text{ mA} > 0.059 \text{ mA}$$

The currents i_C and I_{Cex} can also be compared:

$$i_C = \beta \cdot i_B = 100 \cdot 0.16 \cdot 10^{-3} = 16 \text{ mA}$$

$$16 \text{ mA} > 5.9 \text{ mA}$$

Since $i_B > I_{Bsat}$ and $i_C > I_{Cex}$ (either comparison is sufficient), T cannot be in a_F, meaning T is in *exc*.
In *exc*, the collector current I_C is at the maximum possible value:

$$I_C = I_{Cex} = 5.9 \text{ mA}$$

The collector-emitter voltage V_{CE} in *exc* is:

$$v_{CE} = V_{CEsat} = 0.2 \text{ V}$$

2. For the circuit at **Example 1**, with $V_{CT} = 3.1$ V and $\beta \in (25 \ldots 200)$, determine the range of values of R_B so that T is in:
i) a_F
ii) *exc*.

Solution:
i) T is in a_F for:

$$i_B < \frac{I_{Cex}}{\beta_{max}}$$

$$\frac{V_{CT} - v_{BE}}{R_B} < \frac{V_{PS} - V_{CEsat}}{R_C \cdot \beta_{max}}$$

$$R_B \cdot I_{Cex} > (V_{CT} - v_{BE}) \cdot \beta_{max}$$

$$R_B > \frac{(V_{CT} - v_{BE}) \cdot \beta_{max}}{I_{Cex}}$$

$$R_B > \frac{(3.1 - 0.6) \cdot 200}{5.9 \cdot 10^{-3}}$$

$$R_B > 84.75 \text{ k}\Omega$$

ii) T is in *exc* for:

$$i_B > \frac{I_{Cex}}{\beta_{min}}$$

$$\frac{V_{CT} - v_{BE}}{R_B} > \frac{V_{PS} - V_{CEsat}}{R_C \cdot \beta_{min}}$$

$$R_B \cdot I_{Cex} < (V_{CT} - v_{BE}) \cdot \beta_{min}$$

$$R_B < \frac{(V_{CT} - v_{BE}) \cdot \beta_{min}}{I_{Cex}}$$

When T is in *exc*, the base-emitter voltage is a little bit bigger than $V_{BE,on}$. A value of v_{BE} = 0.8 V is appropriate.

$$R_B < \frac{(3.1 - 0.8) \cdot 20}{5.9 \cdot 10^{-3}}$$

$$R_B < 7.8\ \text{k}\Omega$$

Problems

1. Determine the operating region of T in Fig.5.16, if $V_{BE,on}$ = 0.6 V, β = 100, and R_B = 50 kΩ for the following values of the control voltage V_{CT}:
i) V_{CT} = 0.4 V
ii) V_{CT} = 2.3 V
iii) V_{CT} = 6 V
iv) V_{CT} = 11 V.
Compute the values of I_C and V_{CE} for each case.

2. For the circuit in **Problem 1**, for V_{CT} = 1.9 V and $\beta \in$ (10…150), determine the range of values of R_B so that T is in:
i) a_F
ii) *exc*.

5.5 Enhancement mode MOSFETs

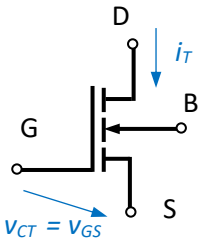
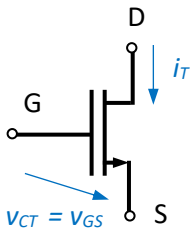
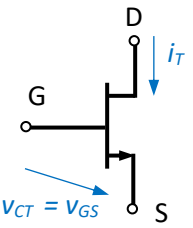
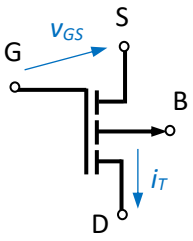
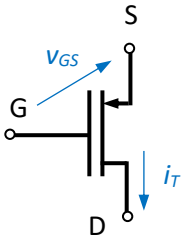
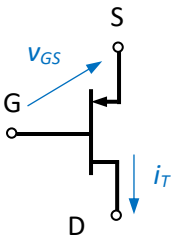
5.5.1 Symbols and physical structure

Field-effect metal-oxide semiconductor transistors (MOSFETs) are the most widely used components in integrated circuits [1]. Their reduced size, compared to the BJTs, makes them the perfect candidate for integration onto a single chip. MOSFETs are built on a semiconductor Silicon substrate (also known as *body*), and the terminals are: *gate* – G, *drain* – D, *source* – S, and *body* – B. The circuit symbols for enhancement mode MOSFETs, *n*-channel and *p*-channel, are shown in Table 5.1, together with the positive directions for the control voltage, v_{GS} and the controlled current, i_T. The arrowhead indicates the source terminal and corresponds to the positive current flow. The space between the two vertical lines in the general symbols and the simplified symbols with explicit channel indicate the isolation between the gate and the body.

MOSFETs are unipolar transistors, the controlled current is due to a single type of carriers that flow through the channel (*n*-type or *p*-type). For n-channel MOSFETs, the current flows through the channel determined by *n*-type carriers.

The simplified physical structure of an enhancement type n-channel MOSFET, denoted NMOS, is shown in Fig.5.17.

Table 5.1. Circuit symbols for enhancement mode MOSFETs

MOSFET	General symbols, explicit body terminal	Simplified symbols, explicit channel	Simplified symbols
n-channel			
p-channel			

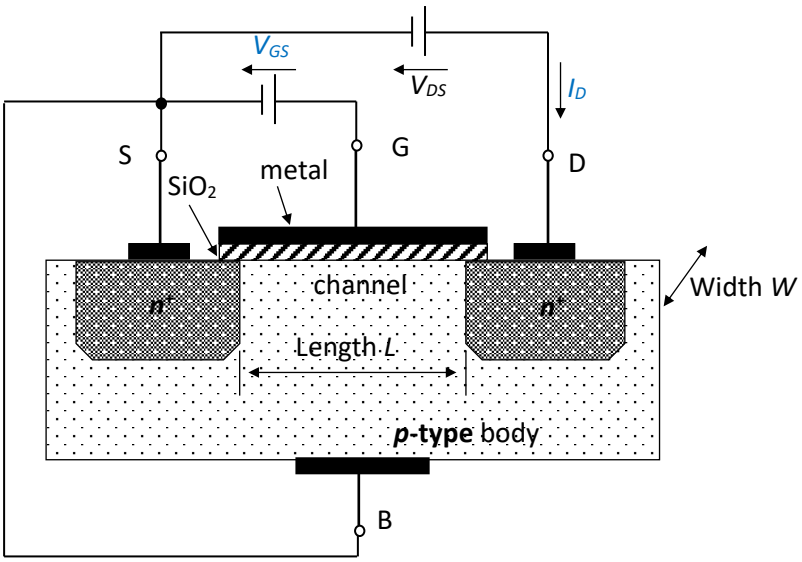


Fig.5.17. NMOS - simplfied physical structure with voltage sources

The NMOS is formed by three layers – metal, Silicon oxide (SiO_2) and a semiconductor substrate or body, which justifies the name of the transistor (MOS – metal oxide semiconductor). Typical values are [1]:

- thickness of the oxide layer t_{ox} = 0.001 to 0.01 µm
- channel length L = 0.03 to 1 µm, which is the distance between drain and source
- channel width W = 0.1 to 100 µm, which is how long the drain and source regions are.

The drain and source regions are heavily doped n^+ regions, while the body is a *p*-type region. The isolation between drain and source is achieved by the Silicon oxide layer, on top of which resides the metal gate G. Metal plates are also present at the other terminals – D, S and B.

The insulating oxide layer between gate and body provides a very high (ideally infinite) input resistance, and the gate current is considered null. The current flows between drain and source through a channel created at the surface of the semiconductor body; this channel must have a reverse polarity compared to the rest of the semiconductor body, that is to be an *n*-type channel. The length *L* and width *W* of this created channel influence the current flowing from drain to source.

5.5.2 Operation and static characteristics

Without any voltage sources connected to the NMOS, two *pn* junctions are present between D and S, like two diodes connected anode to anode: one between body and drain, the other between body and source. When a voltage source V_{DS} is connected between drain and source, there will be no current flow from drain to source, because of the two diodes connected in anti-series. The channel between D and S is formed only as an effect of applying a positive voltage in the gate terminal, and this voltage must be above V_{Thn} ($V_{Thn} > 0$). When more electrons accumulate in the body, below the oxide layer, the channel becomes deeper or is *enhanced*, which explains the name of such MOSFETs. The conductive channel is created and becomes deeper (enhanced) when the electrons accumulate below the oxide layer. The voltage applied in the gate determines the reverse in polarity at the surface of the body, below the oxide layer, and the channel resistivity.

When $v_{GS} < V_{Thn}$, the *n*-type channel between D and S is not created, the NMOS transistor is *off*, and $I_D = 0$ mA.

When $v_{GS} > V_{Thn}$, the NMOS is no longer *off* and the channel between D and S is created (Fig.5.18). Since the source S is connected to ground, the voltage applied in the gate is the gate-source voltage, v_{GS}. At the beginning, the positive v_{GS} rejects the holes in the gate region and attracts the electrons from the drain and source regions. These electrons accumulate under the oxide layer, in the gate region.

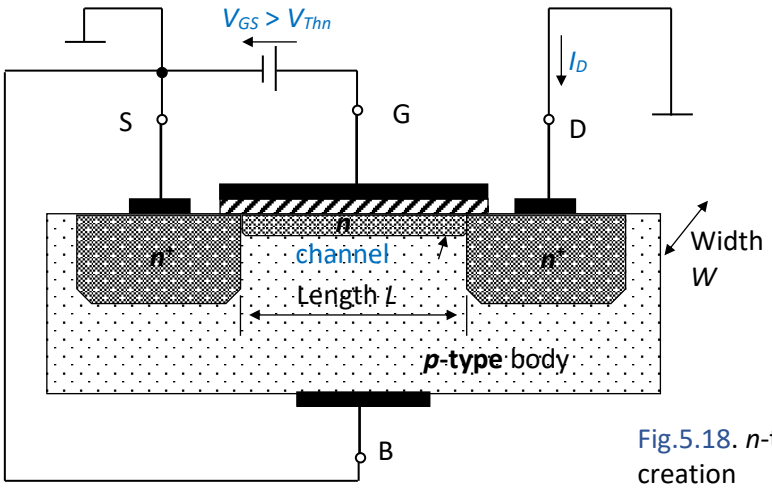


Fig.5.18. *n*-type channel creation

The channel between D and S is formed when enough electrons accumulate at the surface of the body, so that a current can flow from D to S, when a voltage source $V_{DS} > 0$ is connected to the transistor.

$$V_{GS} > V_{Thn}$$
$$V_{DS} = 0 \text{ V}$$
$$I_D = 0 \text{ mA}$$

When $V_{DS} > 0$ V, the current $I_D > 0$ mA flows through the channel; the value of the current depends on (V_{GS} -V_{Thn}) and on V_{DS}. The voltage drop between G and S is V_{GS}, while the voltage drop between G and D is $V_{GD} = V_{GS} - V_{DS} < V_{GS}$. Consequently, the channel has different widths at its ends: the channel is wider at the source region and shallower at the drain region – Fig.5.19. The channel is shallower at the drain end because the positive drain region attracts the electrons in its vicinity. The transistor operates in the linear region, where the control voltage V_{GS} and the controlled current I_D have a linear dependency. The equations that describe the behaviour of the transistor in this operating region are:

$$V_{GS} > V_{Thn}$$
$$0 \text{ V} < V_{DS} < V_{DSsat}$$
$$V_{DSsat} = V_{GS} - V_{Thn}$$
$$I_D > 0 \text{ mA}$$
$$I_D = \beta \cdot \left[2 \cdot (V_{GS} - V_{Thn}) \cdot V_{DS} - V_{DS}^2\right]$$
$$I_D = \frac{K}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot (V_{GS} - V_{Thn}) \cdot V_{DS} - V_{DS}^2\right]$$
$$\beta = \frac{K}{2} \cdot \frac{W}{L}$$

where:

- β [µA/V^2] – constructive parameter of the transistor
- K [µA/V^2] – transconductance parameter, depends on the mobility of the free carriers and on the capacitance of the oxide layer
- W and L [µm] – physical dimensions of the conducting channel.

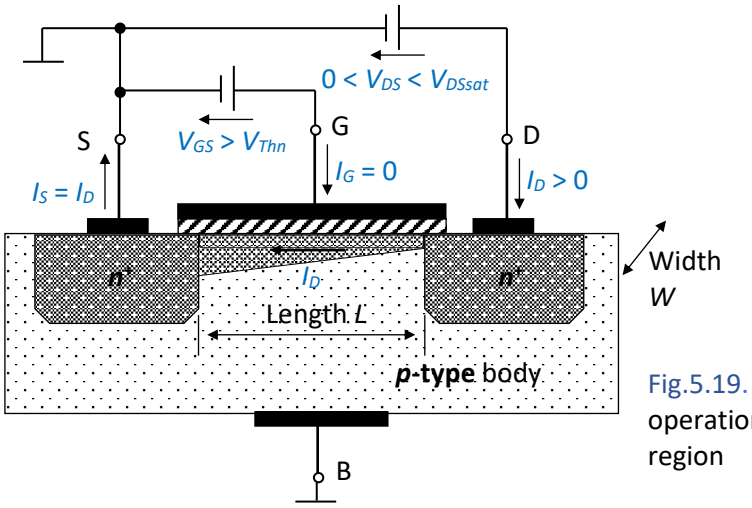


Fig.5.19. NMOS operation in the linear region

When V_{DS} reaches the saturation value V_{DSsat}, the voltage applied between G and D is $V_{GD} = V_{GS} - V_{Dssat} = V_{Thn}$. The channel depth becomes null at the drain end (Fig.5.20). The drain current I_D is almost constant and limited to a superior value, for a given V_{GS}. Even if V_{DS} increases and exceeds V_{DSsat}, the drain current remains constant and no longer depends on V_{DS}. The transistor now operates in the *pinch-off* or *saturation* or *active* region. Even though the channel is pinched-off, it allows the current I_D to flow, and this current is constant. In this operating region, the controlled current varies with the square of the control voltage:

$$V_{GS} > V_{Thn}$$
$$V_{DS} > V_{DSsat}$$

$$V_{DSsat} = V_{GS} - V_{Thn}$$

$$I_D > 0 \text{ mA}$$

$$I_D = \beta \cdot (V_{GS} - V_{Thn})^2 \cdot (1 + \frac{V_{DS}}{V_A}) \approx \beta \cdot (V_{GS} - V_{Thn})^2$$

$$I_D = \frac{K}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{Thn})^2 \cdot (1 + \frac{V_{DS}}{V_A}) \approx \frac{K}{2} \cdot \frac{W}{L} (V_{GS} - V_{Thn})^2$$

$$\beta = \frac{K}{2} \cdot \frac{W}{L}$$

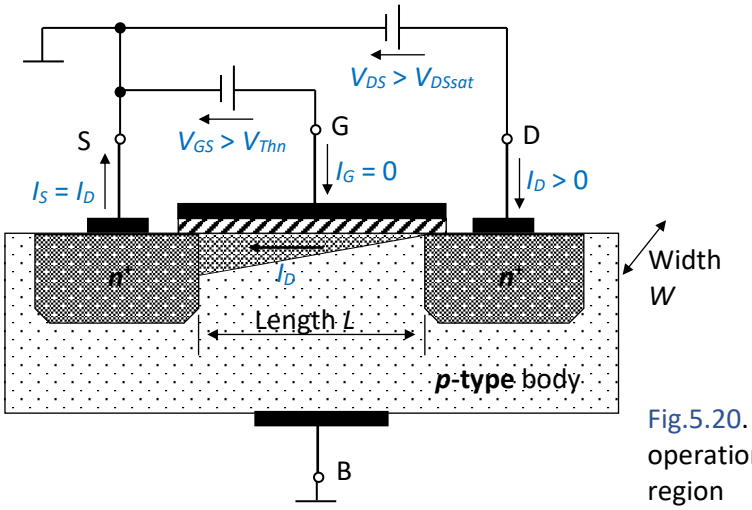


Fig.5.20. NMOS operation in the active region

The equations that involve β are used for discrete transistors (β is found in the datasheet of the transistor), while the equations with W/L and $K/2$ are used for integrated transistors.

The output characteristic $i_D(v_{DS})$ of the NMOS for a fixed value of the control voltage V_{GS} is depicted in Fig.5.21. Note the limitation of the current when the NMOS operates in the active (saturation) region.

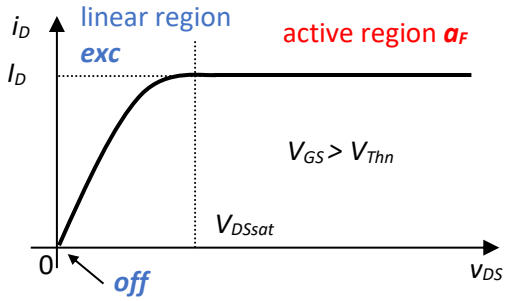


Fig.5.21. NMOS output characteristic $i_D(v_{DS})$

With several different control voltages, the family of output characteristics $i_D(v_{DS})$ with V_{GS} as a parameter is obtained – Fig.5.22. a). The boundary between the linear and active operating regions is given by the v_{Dssat} curve (dotted line). In the linear region, $v_{GD} > V_{Thn}$, while in the active region, $v_{GD} < V_{Thn}$.

$$v_{GD} = v_{GS} - v_{GSsat} = v_{GS} - v_{GS} + V_{Thn} = V_{Thn}$$

The operating regions of the MOSFET are easily distinguishable in Fig.5.22. a):

- *cut-off* region (*off*), represented by the horizontal axis v_{DS}, where $i_D = 0$, regardless of v_{DS}
- *linear* region *exc*, where i_D is a linear function of v_{GS}

- *active forward* region or *saturation* region a_F, where i_D is a square function of v_{GS}.

There is a fourth operating region, active reverse a_R, where the roles of the D and S terminals are reversed. In a_R, the transistor can work as an amplifier, but exhibits poor performance compared to a_F, thus the transistor is rarely set to work in this region. It is recommended to bias the transistor not too close to the boundaries between operating regions.

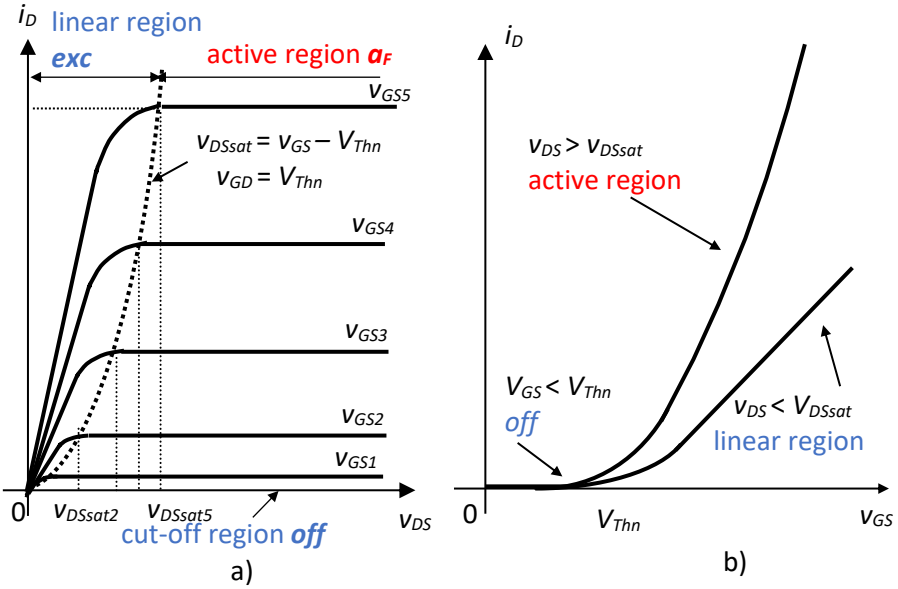


Fig.5.22. NMOS static characteristics
a) output characteristics $i_D(v_{DS})$; b) transfer characteristics $i_D(v_{GS})$.

Two static transfer characteristics $i_D(v_{GS})$ are depicted in Fig.5.22. b). In the active region, where $v_{DS} > V_{Dssat}$, the drain current i_D is a square function of $(v_{GS} - V_{Thn})$. Since the gate current is always null, no other static characteristics can be determined.

To conclude, the operating regions of the NMOS are:

- *cut-off* (*off*), where the NMOS works as an open switch:

$$v_{GS} < V_{Thn}$$
$$I_D = I_S = 0 \text{ mA}$$

- *linear* or *saturation* (*exc*), where the NMOS works as a closed switch

$$v_{GS} > V_{Thn};\ 0\text{ V} < V_{DS} < V_{DSsat}$$
$$I_D = \beta \cdot \left[2 \cdot (V_{GS} - V_{Thn}) \cdot V_{DS} - V_{DS}^2\right]$$

- *active forward* or *saturation* a_F, where the NMOS works as an amplifier:

$$v_{GS} > V_{Thn};\ V_{DS} > V_{DSsat}$$
$$I_D = \beta \cdot (V_{GS} - V_{Thn})^2$$

Additionally, the NMOS can be used as a voltage-controlled linear resistor, when operating in the linear region with low V_{DS}. The higher the v_{GS}, the lower the r_{DS}:

$$v_{GS} > V_{Thn};\ \text{low}\ V_{DS}$$
$$I_D = \beta \cdot \left[2 \cdot (V_{GS} - V_{Thn}) \cdot V_{DS} - V_{DS}^2\right]$$
$$r_{DS} = \frac{v_{DS}}{i_D} = \frac{1}{\beta \cdot \left[2 \cdot (V_{GS} - V_{Thn}) - V_{DS}\right]}$$

$$r_{DS} \approx \frac{1}{2 \cdot \beta \cdot (V_{GS} - V_{Thn})}$$

No resistors were explicitly included when determining the static characteristics of the NMOS. The current through the control terminal G is negligible and approximated to zero, so no resistors are needed in the gate. However, limiting the drain current requires a resistor in the drain (Fig.5.23) or in the source.

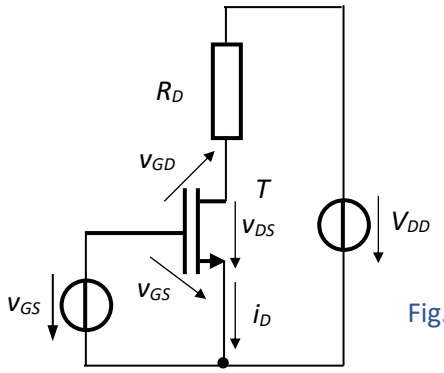


Fig.5.23. NMOS circuit

Examples

1. Determine the operating region of the NMOS transistor in Fig.5.23, for V_{DD} = 12 V, V_{Thn} = 1.4 V, β = 2 mA/V^2, R_D = 4 kΩ, and the following values of V_{GS}:
i) V_{GS} = 1 V
ii) V_{GS} = 2 V
iii) V_{GS} = 6 V.
Compute I_D and V_{DS} for each of the above cases.

Solution:
i) Since $V_{GS} < V_{Thn}$, T is *off*.

$$I_D = 0 \text{ mA}$$
$$V_{DS} = V_{DD} - I_D \cdot R_D$$
$$V_{DS} = V_{DD}$$

ii) $V_{GS} > V_{Thn}$, so T is *on,* in either a_F or *exc*. It's more convenient to assume T is in a_F and determine I_D based on V_{GS} (simpler equation):

$$I_D = \beta \cdot (V_{GS} - V_{Thn})^2$$
$$I_D = 2 \cdot 10^{-3} \cdot (2 - 1.4)^2 = 0.72 \text{ mA}$$
$$V_{DSsat} = V_{GS} - V_{Thn} = 0.6 \text{ V}$$
$$V_{DS} = V_{DD} - I_D \cdot R_D$$
$$V_{DS} = 12 - 0.72 \cdot 10^{-3} \cdot 4 \cdot 10^{3} = 9.12 \text{ V}$$

The computed V_{DS} is compared to $V_{DSsat,}$ to check whether T is in a_F.

$$V_{DS} > V_{DSsat}$$
$$9.12 \text{ V} > 0.6 \text{ V}$$

The criterion is met, meaning T is in a_F for V_{GS} = 2 V. The values for I_D and V_{DS} are:

$$I_D = 0.72 \text{ mA}$$
$$V_{DS} = 9.12 \text{ V}$$

iii) Using the same steps as for ii):

$$I_D = \beta \cdot (V_{GS} - V_{Thn})^2$$
$$I_D = 2 \cdot 10^{-3} \cdot (6 - 1.4)^2 = 42.32 \text{ mA}$$
$$V_{DSsat} = V_{GS} - V_{Thn} = 4.6 \text{ V}$$
$$V_{DS} = V_{DD} - I_D \cdot R_D$$
$$V_{DS} = 12 - 42.32 \cdot 10^{-3} \cdot 4 \cdot 10^3 < 0 \text{ V}$$

The computed V_{DS} is below 0 V, meaning the assumption that T is in a_F was incorrect. For $V_{GS} = 6$ V, T operates in *exc.*

The values for I_D and V_{DS} are determined using the equations for T in *exc.* The maximum value of V_{DS} is:

$$V_{DS} = V_{DSsat} = V_{GS} - V_{Thn} = 4.6 \text{ V}$$
$$I_D = \beta \cdot \left[2 \cdot (V_{GS} - V_{Thn}) \cdot V_{DS} - V_{DS}^2\right]$$

$$I_D = 2 \cdot 10^{-3} \cdot \left[2 \cdot (6 - 1.4) \cdot 4.6 - 4.6^2\right]$$
$$I_D = 42.32 \text{ mA}$$

The same value of I_D would have been obtained using the equation for T in a_F, because the value of V_{DS} was assumed to be maximum (V_{DSsat}), meaning the boundary between the two operating regions, a_F and *exc*.

2. For the circuit in **Example 1**, find the maximum value of V_{GS} for which T works in a_F.

Solution:

The boundary between a_F and *exc* is given by

$$V_{DS} = V_{DSsat} = V_{GS} - V_{Thn}$$

The current I_D can be determined using either the equation for T in a_F or *exc*.

$$V_{DS} = V_{DD} - I_D \cdot R_D$$
$$V_{DSsat} = V_{GS} - V_{Thn}$$
$$V_{DD} - I_D \cdot R_D = V_{GS} - V_{Thn}$$
$$I_D = \beta \cdot (V_{GS} - V_{Thn})^2$$
$$V_{DD} - \beta \cdot (V_{GS} - V_{Thn})^2 \cdot R_D = V_{GS} - V_{Thn}$$

The unknown is V_{GS}:

$$12 - 2 \cdot 10^{-3} \cdot (V_{GS} - 1.4)^2 \cdot 4 \cdot 10^3 = V_{GS} - 1.4$$

Let $y = V_{GS} - 1.4$:

$$12 - 8 \cdot y^2 = y$$
$$8 \cdot y^2 + y - 12 = 0$$
$$\Delta = 385$$
$$y_{1,2} = \frac{-1 \pm 19{,}62}{-16}$$
$$y_1 = -1.28$$
$$y_2 = 1.16$$

The first solution is discarded (it would result in $V_{GS} < V_{Thn}$).

The maximum value of V_{GS} for which T operates in a_F is $V_{GSmax} = 2.56$ V.

The computed value is checked in the other equations for in a_F:

$$I_D = \beta \cdot (V_{GS} - V_{Thn})^2$$
$$I_D = 2 \cdot 10^{-3} \cdot (2.56 - 1.4)^2 = 2.71 \text{ mA}$$

$$V_{DSsat} = 2.56 - 1.4 = 1.16 \text{ V}$$
$$V_{DS} = V_{DD} - I_D \cdot R_D$$
$$V_{DS} = 12 - 2.71 \cdot 10^{-3} \cdot 4 \cdot 10^{3} = 1.16 \text{ V}$$

The values of V_{DS} and V_{DSsat} are equal, proving that the computed value of V_{GS} is indeed correct.
Note that **Example 1** can also be solved by comparing the given values of V_{GS} with the maximum value for which T works in a_F, that is V_{GSmax}:
i) V_{GS} = 1 V – T is *off*, $V_{GS} < V_{Thn}$
ii) v_{GS} = 2 V – T is in a_F, $V_{Thn} < V_{GS} < V_{GSmax}$
iii) v_{GS} = 6 V - T is in *exc*, $V_{GS} > V_{Thn}$ and $V_{GS} > V_{GSmax}$.

Problems

1. Determine the operating region of the NMOS transistor in Fig.5.23, for V_{DD} = 15 V, V_{Thn} = 1.2 V, β = 1.4 mA/V^2, R_D = 2 kΩ, and the following values of V_{GS}:
i) V_{GS} = 0.8 V
ii) V_{GS} = 1.7 V
iii) V_{GS} = 2.2 V
iv) V_{GS} = 8 V.
Compute I_D and V_{DS} for each of the above cases.

2. For the circuit in **Problem 1**, find the maximum value of V_{GS} for which T works in a_F.

3. Find the minimum value of V_{GS} for which the NMOS transistor in Fig.5.23 operates in *exc,* for V_{DD} = 18 V, V_{Thn} = 2 V, β = 1.4 mA/V^2, R_D = 5 kΩ.
Determine the operating region for V_{GS} = 3.2 V. Propose a method to obtain V_{GS} = 3.2 V using a resistive divider out of V_{DD}. Size the newly added components.

References

[1] Sedra, A.S., Smith, K.C., Microelectronic Circuits, 6th Edition, Oxford University Press, ISBN-10: 0195323033, 2010

[2] Oltean, G., Electronic Devices, Editura UTPress, Cluj-Napoca, ISBN 973-662-220-7, 2006

[3] Feștilă, Lelia, Circuite integrate analogice II, Casa Cărții de Știință, Cluj-Napoca, 1999

[4] Oltean, G., Şipoş, Emilia, Oltean, Ioana, A new approach of op-amp amplifier biasing, Buletinul Științific al Universității "Politehnica", Timișoara, Oct. 2004, Tom 49(63), Fascicola 2, ISSN 1224-6034, pag. 328-331

[5] Oltean, G., Gordan, Mihaela, Oltean, Ioana, A new method to deduce the voltage transfer characteristic for some two-port networks, Acta Technica Napocensis Electronics and telecommunications, vol.40, no.2, 2000, pag. 17-20

[6] Moore, G, Cramming More Components onto Integrated Circuits, Proc. IEEE, vol. 86 (1), January 1998
https://www.cs.utexas.edu/~fussell/courses/cs352h/papers/moore.pdf

[7] How many Transistors in a CPU? April 2020
https://www.utmel.com/blog/categories/transistors/how-many-transistors-in-a-cpu

[8] Apple Press Release January 2023
Apple unveils MacBook Pro featuring M2 Pro and M2 Max - Apple (RO)

[9] Horowitz, P., Hill, W., The art of Electronics, Second edition, Cambridge University Press, ISBN-10: 0521370957, 1997